

LENOVO FAB#: LJ406

lenovo 联想

LENOVO.CRDN

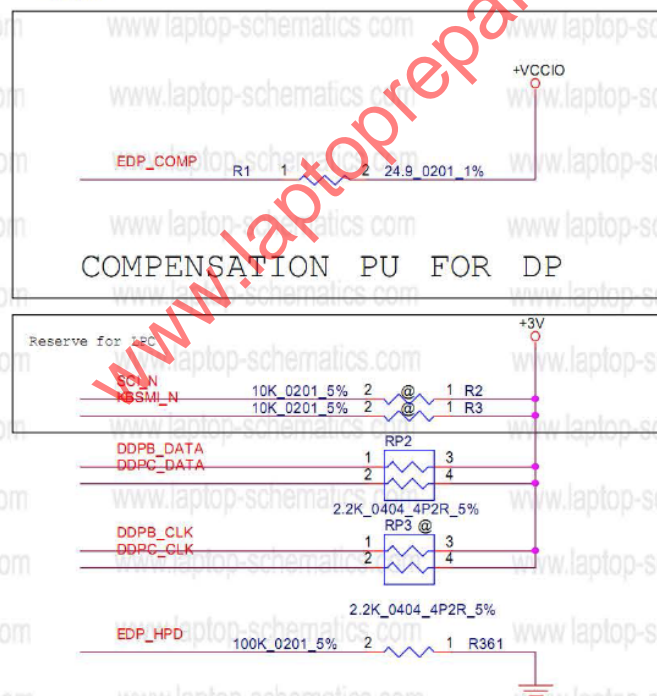
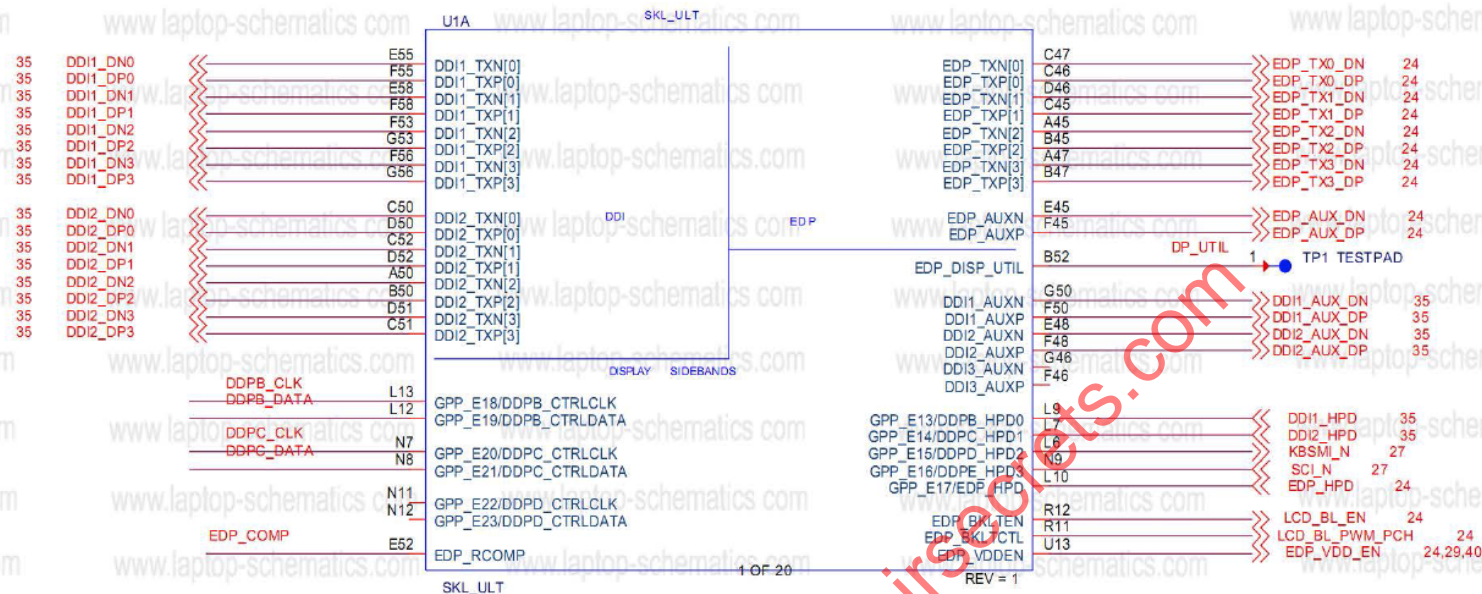
Block Diagram

Rev: 1.0

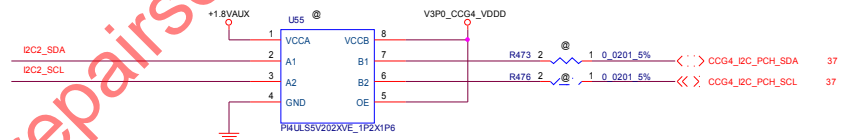
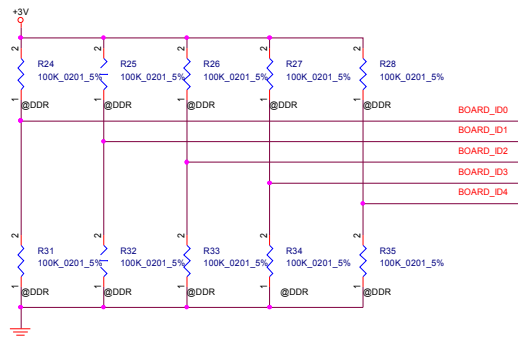
YOGA930

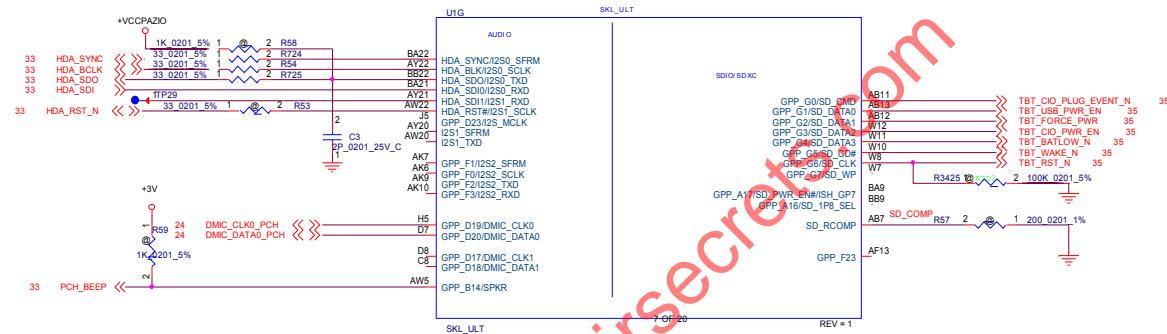
Wednesday, June 13, 2018

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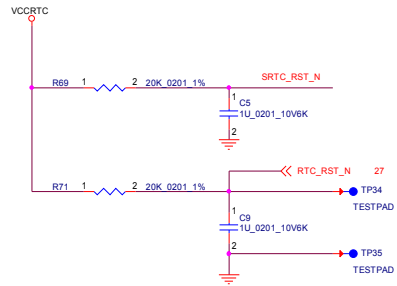
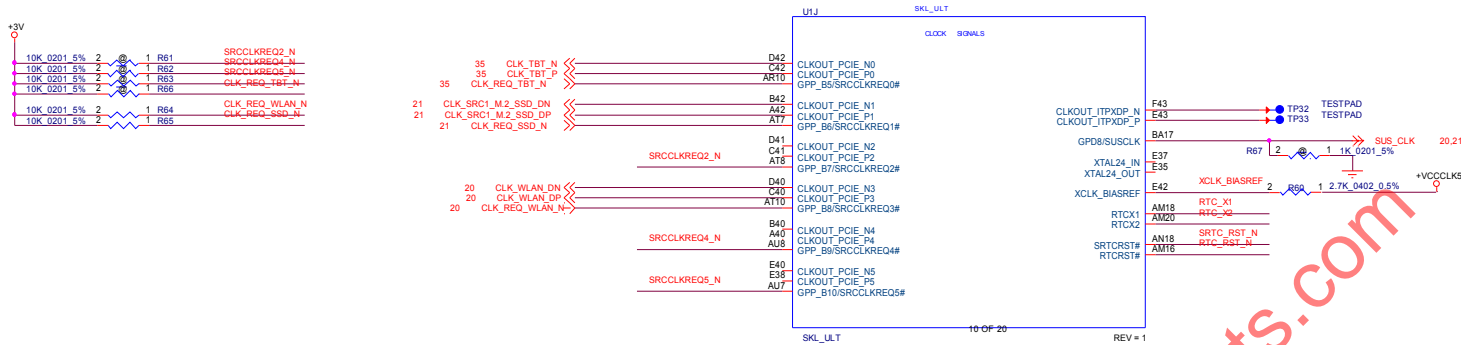
LENOVO FAB#: IJ406	
lenovo 联想	
LENOVO.ORDN	
Kaby Lake MCP (DDI,EDP)	
YOGA930	Rev1.0
Date: Wednesday, June 13, 2018	Sheet: 2 of 50
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LENOVO.CRDN			
Title Kaby Lake MCP (HDA/I2S/SDIO/DMIC)			
Size	Document Number	Rev	
C	YOGA930	V1.0	
Date: Wednesday, June 13, 2018 Sheet 6 of 50			
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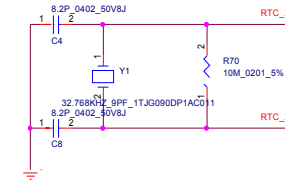
Any un-used SRCCLKREQ# signal not mapped to a Down Device or Connector/ADD-In Card must be disabled using the Kaby Lake Platform FTT tool and they must be left as no connects at the CPU side on the platform



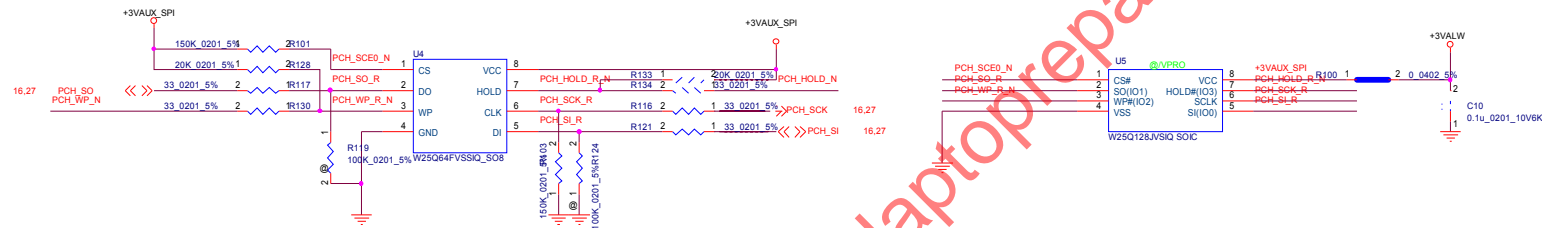
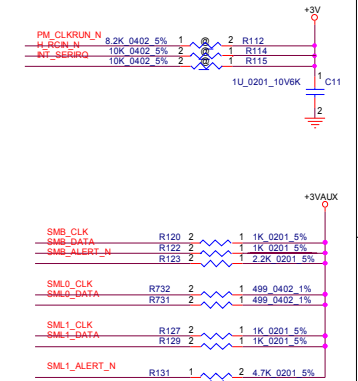
ME RESET
SAVE ME = PU (Default)
CLEAR ME = PD

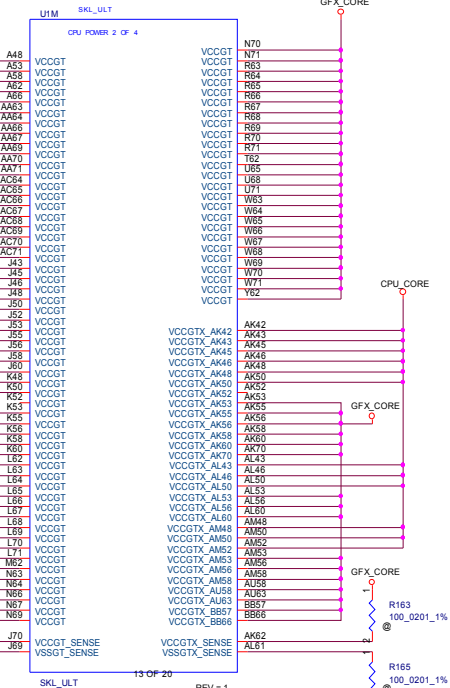
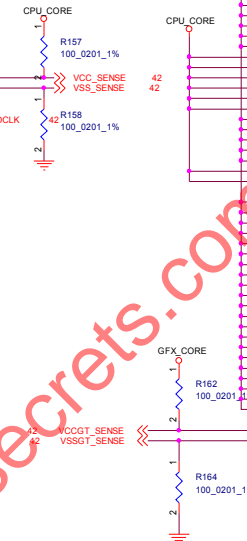
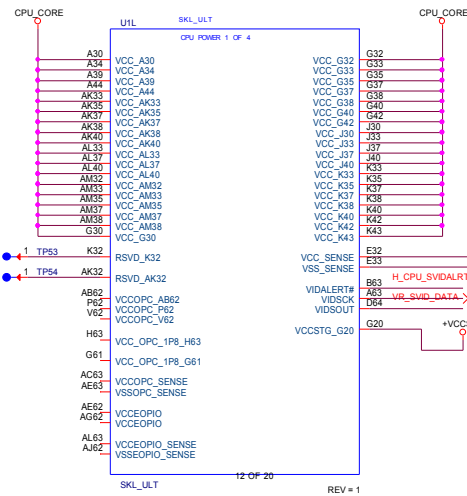
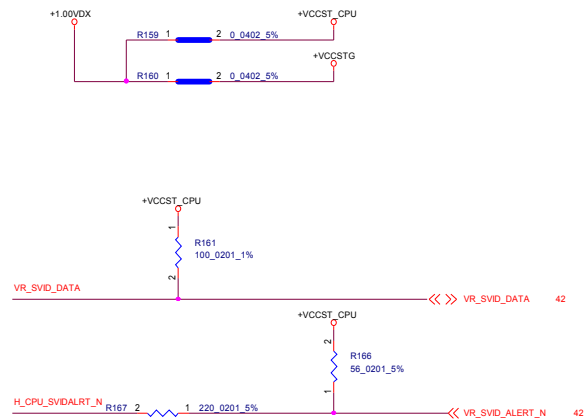
CMOS RESET
SAVE CMOS = PU (Default)
CLEAR CMOS = PD

TP34 TP35 Need to put on the TOP

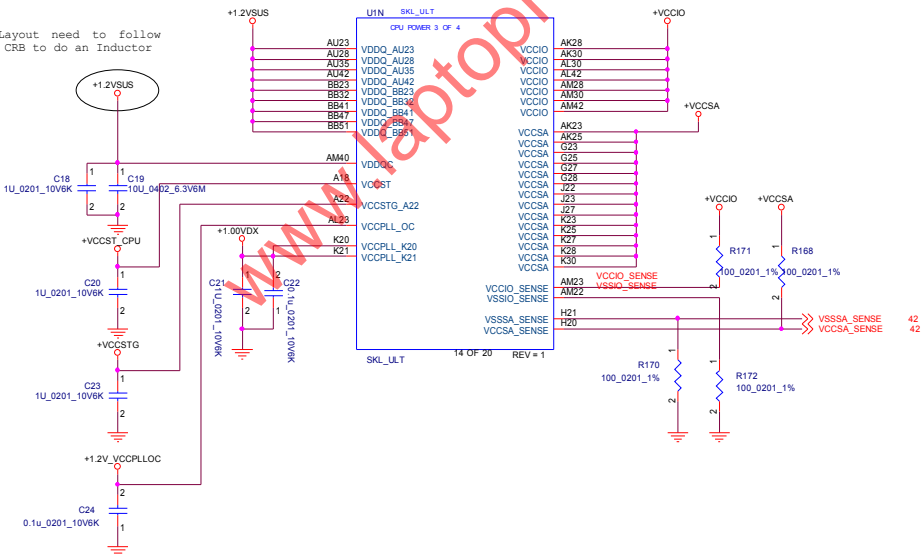


LENOVO.CRDN			
Kaby Lake MCP (CLK)			
Size C	Document Number	RevV1.0	
YOGA930			
Date:	Wednesday, June 13, 2018	Sheet	7 of 50
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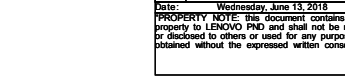
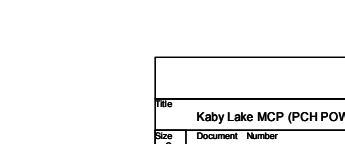
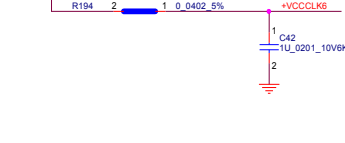
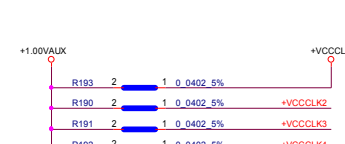
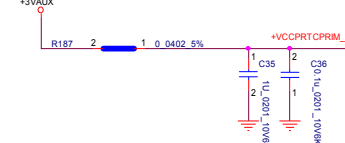
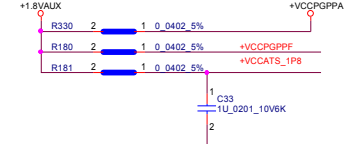
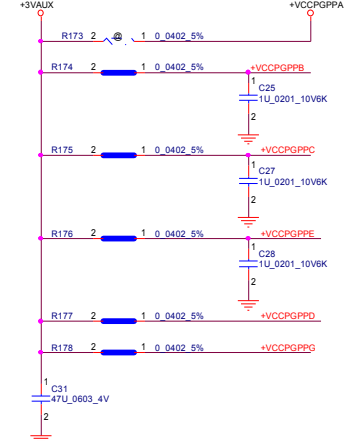
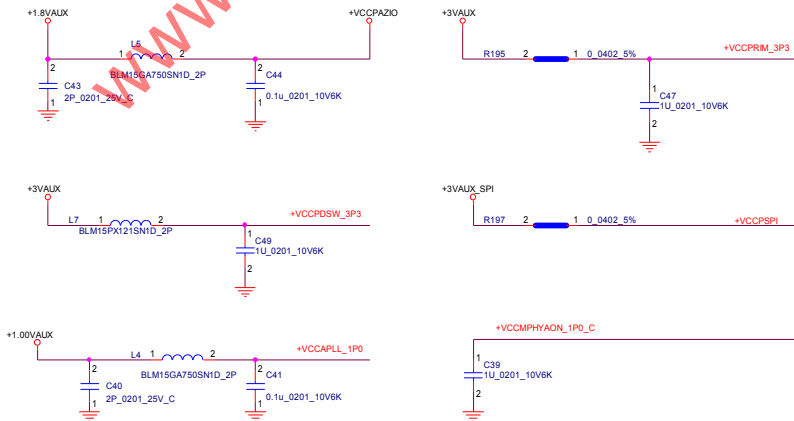
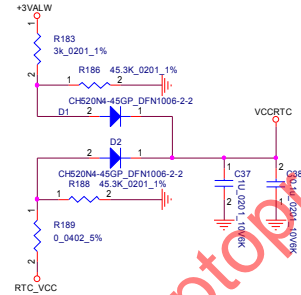
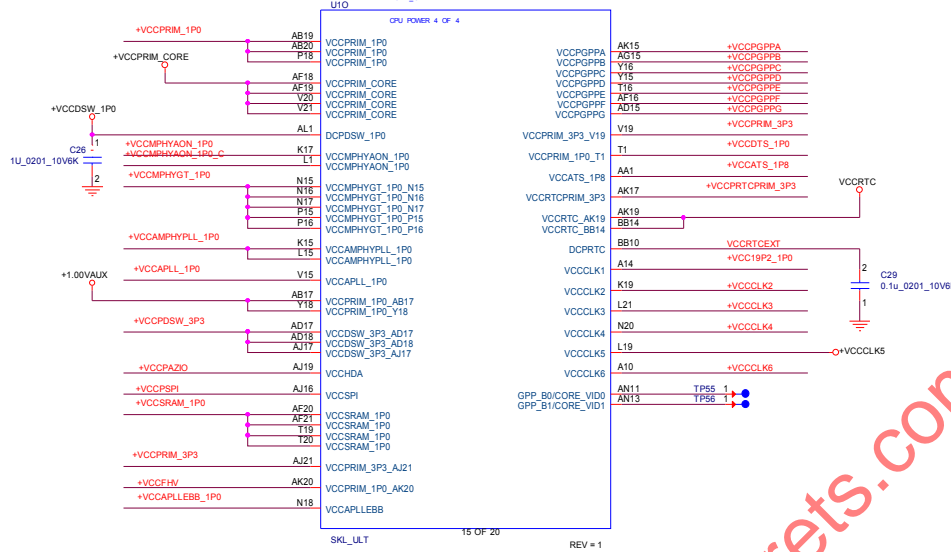
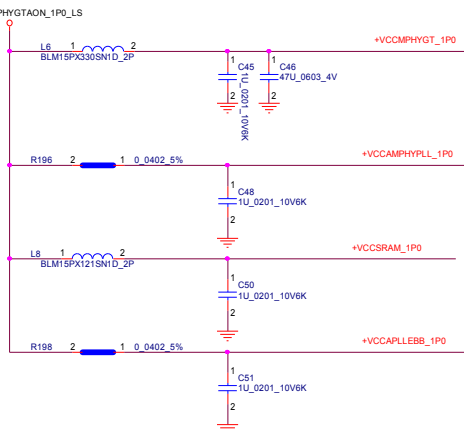
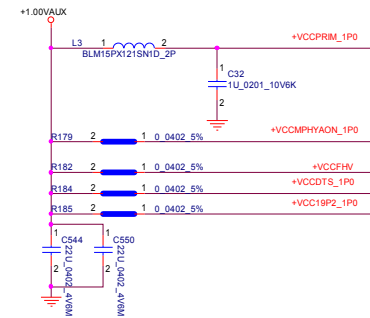
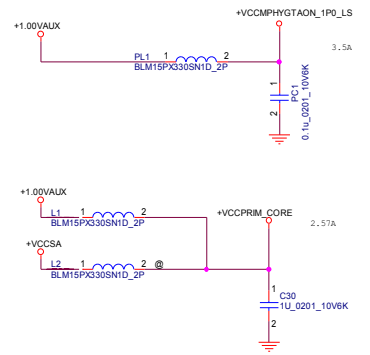




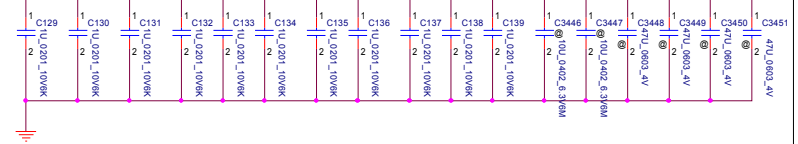
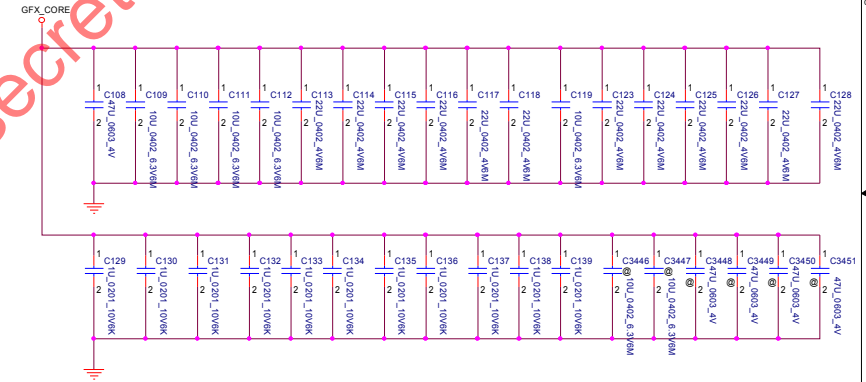
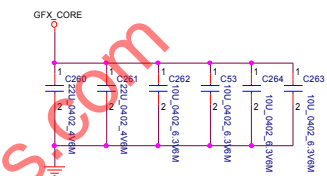
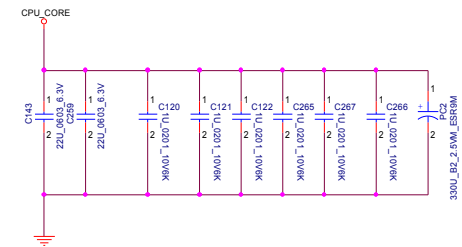
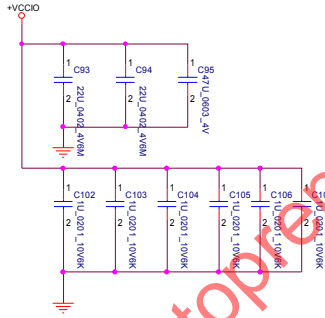
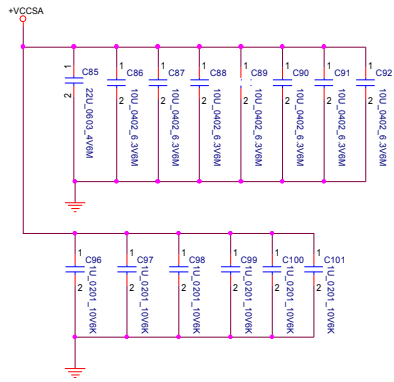
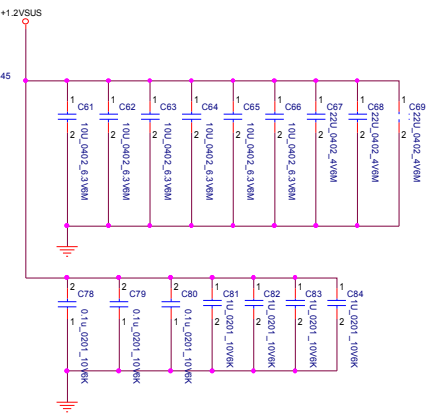
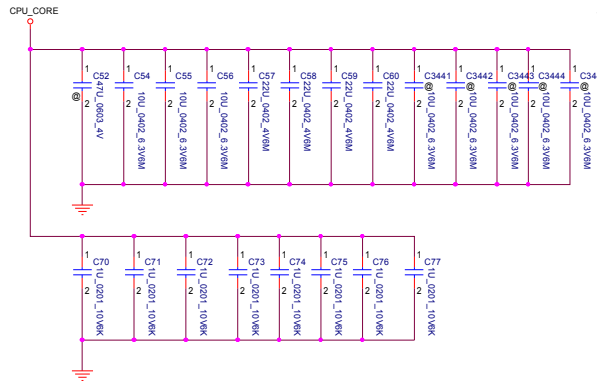
Note: Layout need to follow CRB to do an Inductor



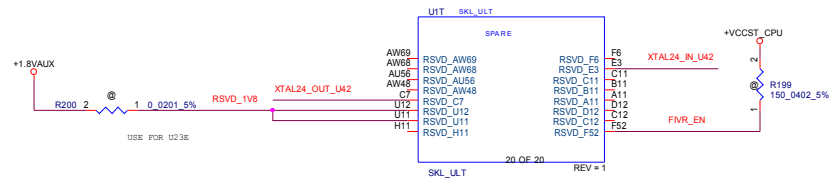
LENOVO.CRDN			
Kaby Lake MCP (PROCESSOR POWER)			
Size	Document Number	Rev1.0	
C	YOGA920		
Date:	Wednesday, June 13, 2018	Sheet	11 of 50
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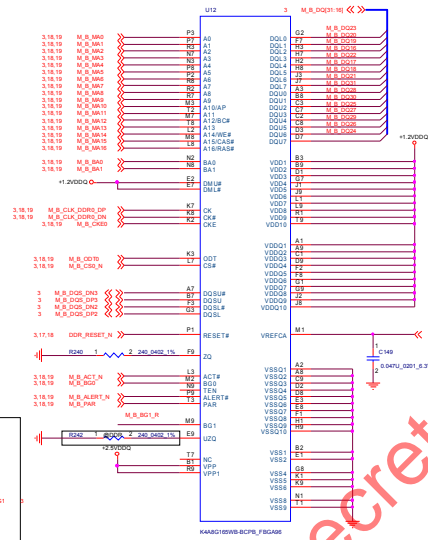
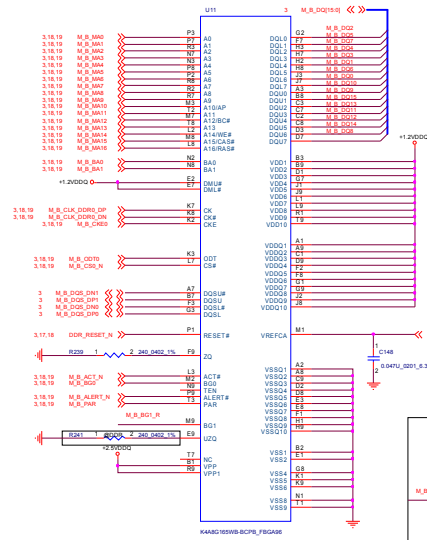


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Kaby Lake MCP (PCH POWER)			
Size	Document Number	Rev1.0	
C	YOGA930		
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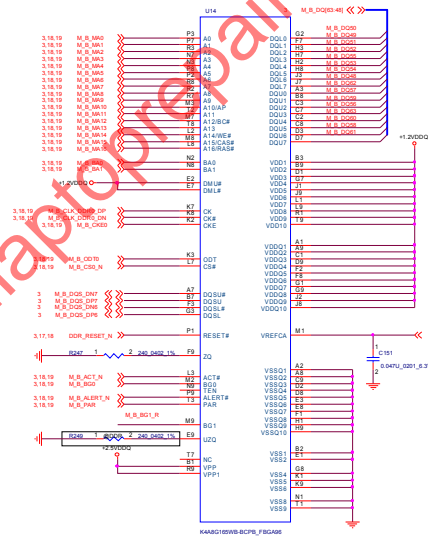
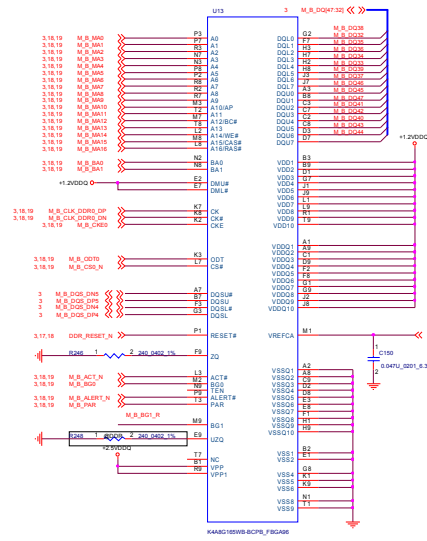


LENOVO.CRDN			
File	Kaby Lake MCP (Power CAP)		
Doc	Document Number	RevV1.0	
C	YOGA930		
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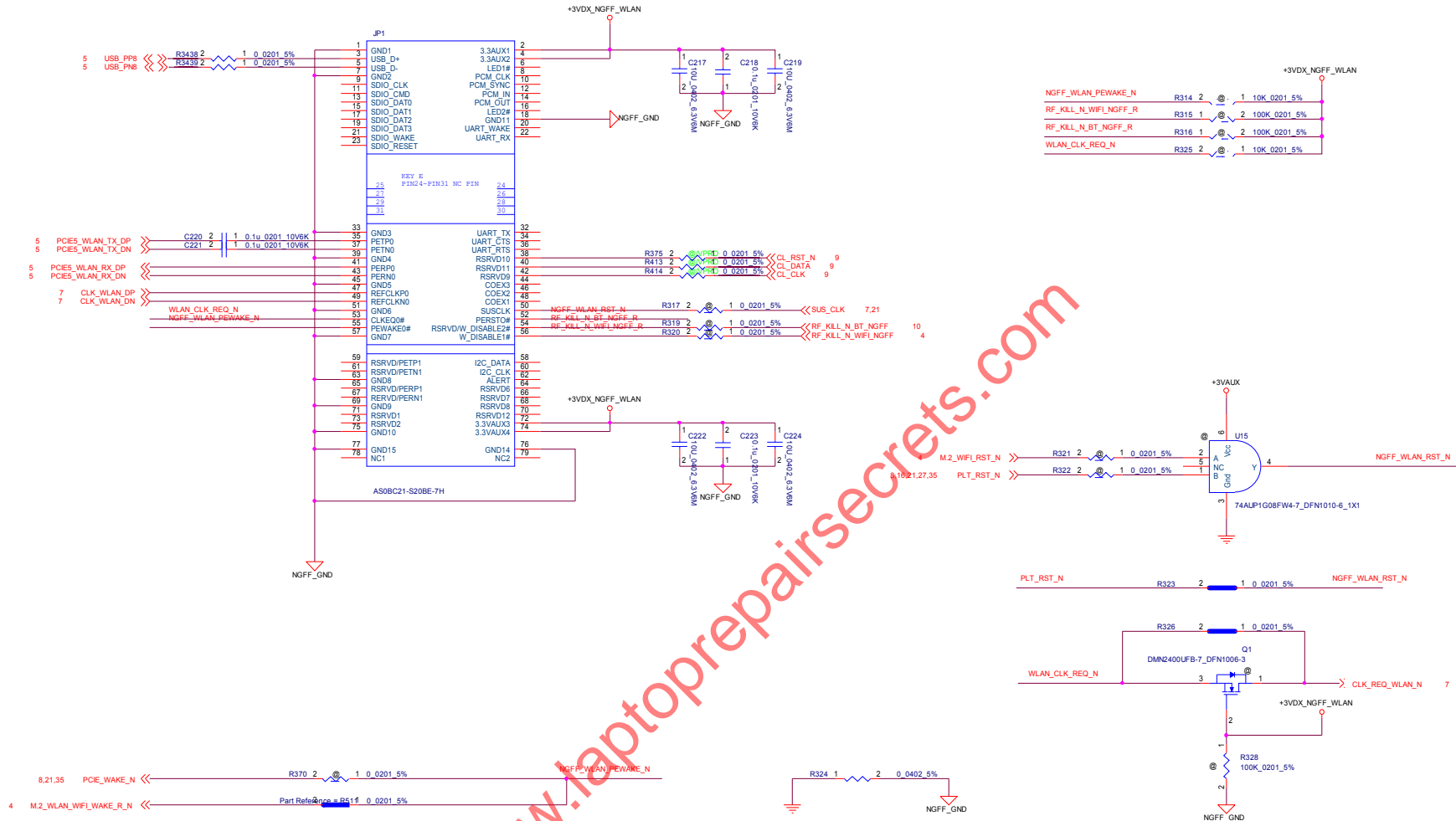




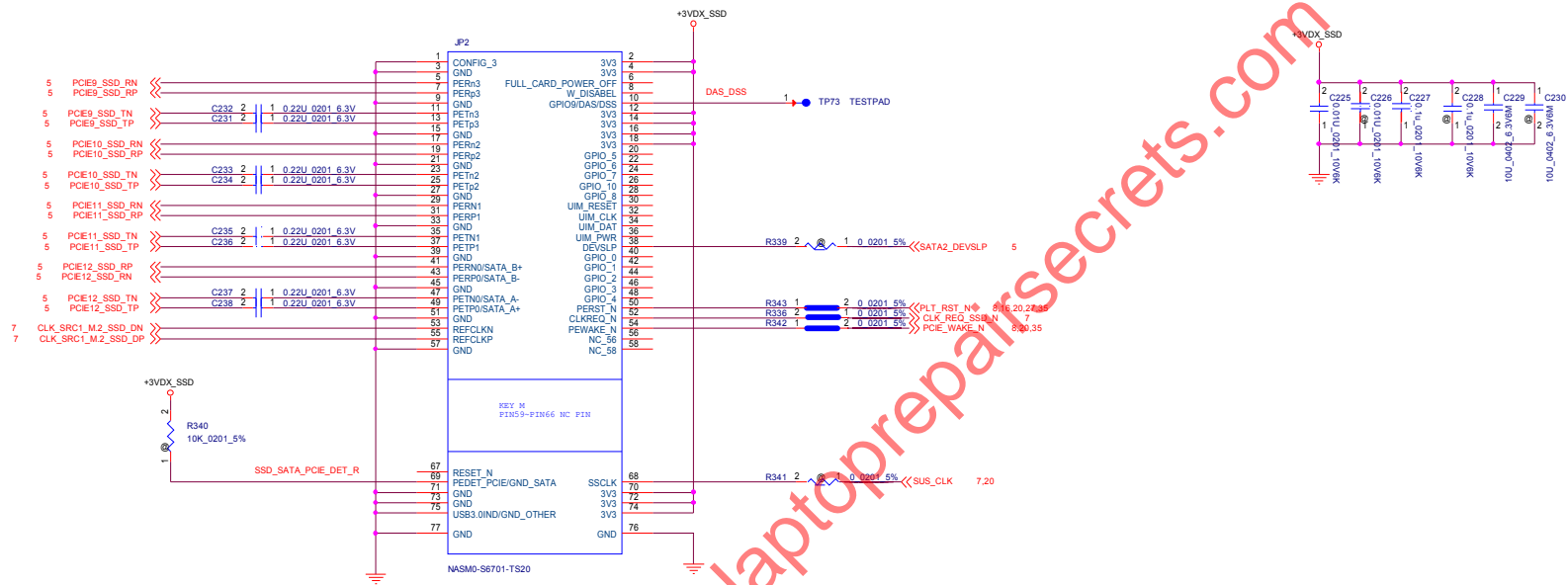
DDP: Stuff R244 and R243, Dummy R245; R241 242 248 249 @ 240ohm
SDP: Dummy R244 and R243, Stuff R245; R241 242 248 249@ 0ohm



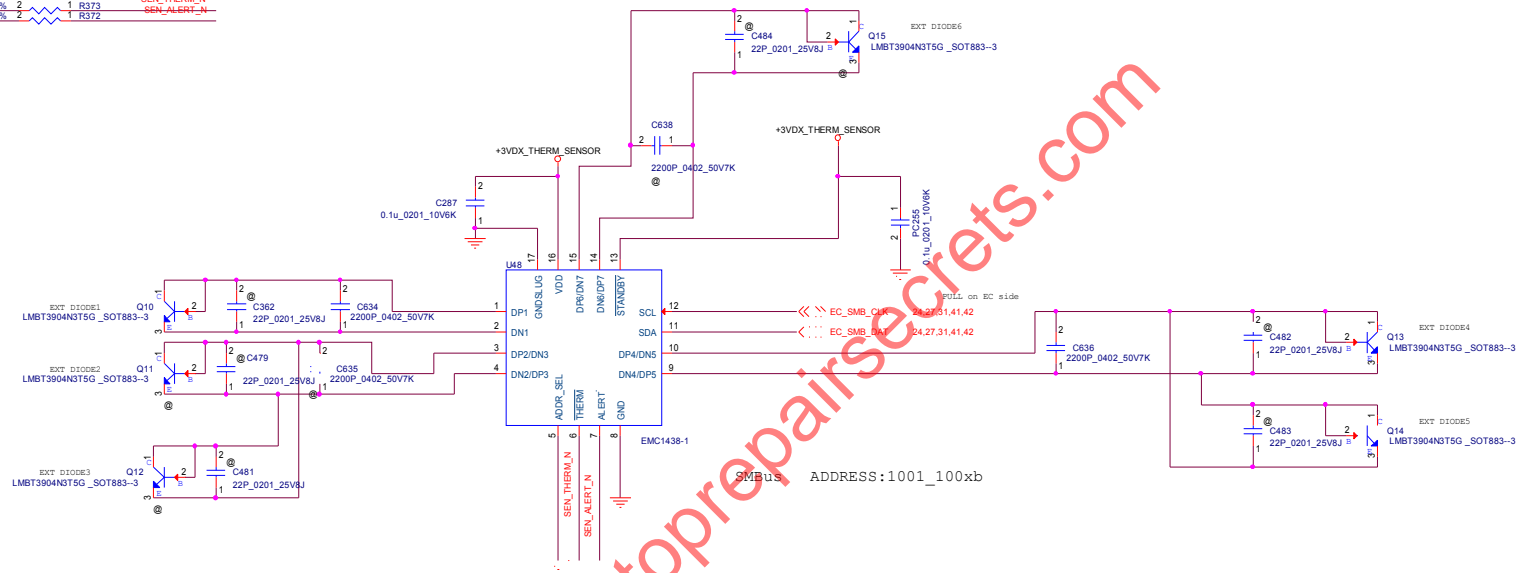
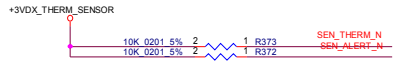
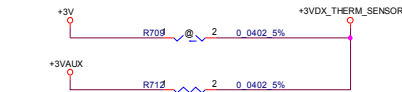
LENOVO CRDN			
DDR4-ONBD			
Rev D	Rev C	Rev B	Rev A
YOGA330	YOGA330	YOGA330	YOGA330
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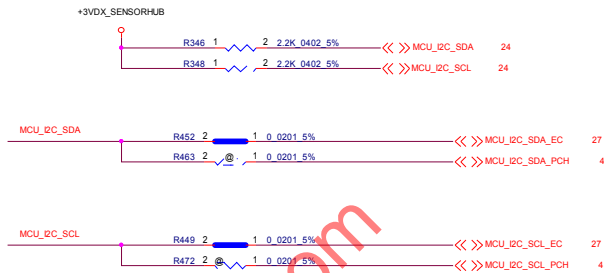
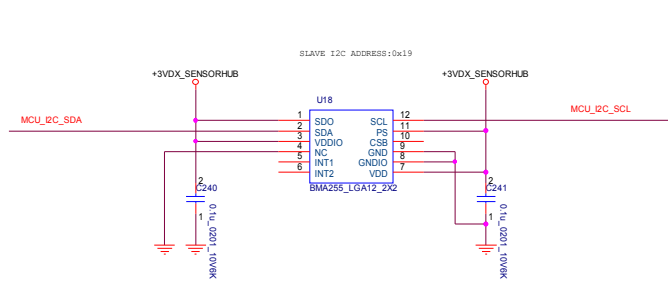
LENOVO.CRDN			
NGFF WLAN			
Size	Document Number	RevV1.0	
C	YOGA930		
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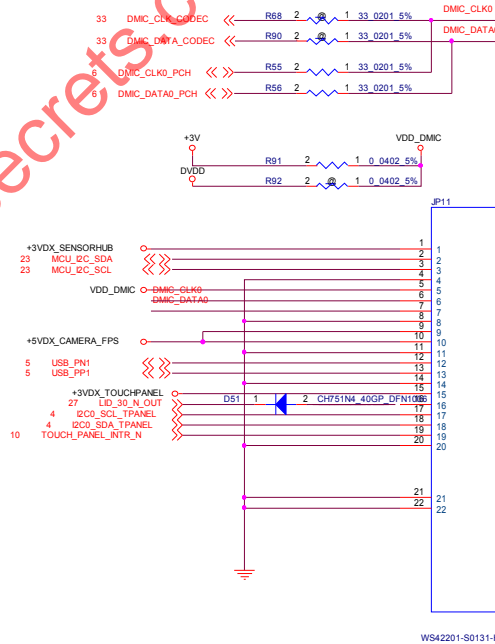
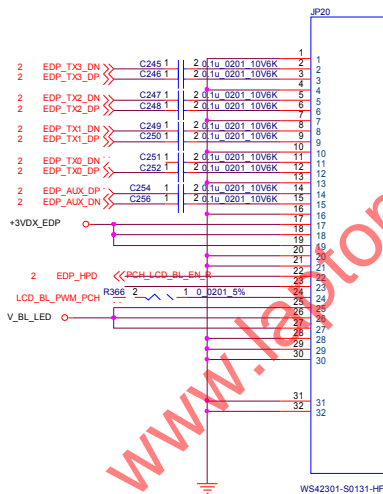
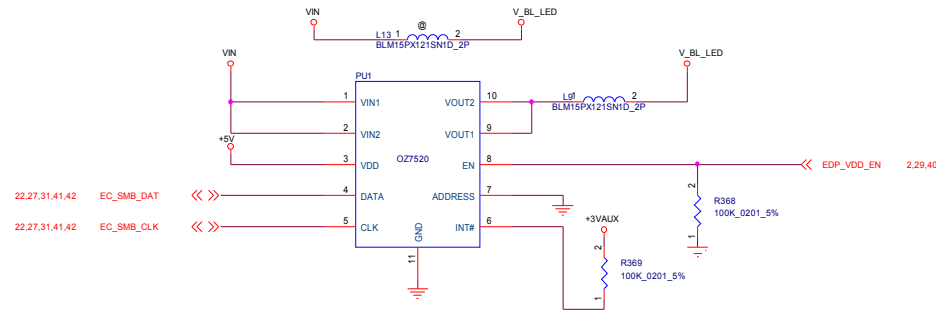
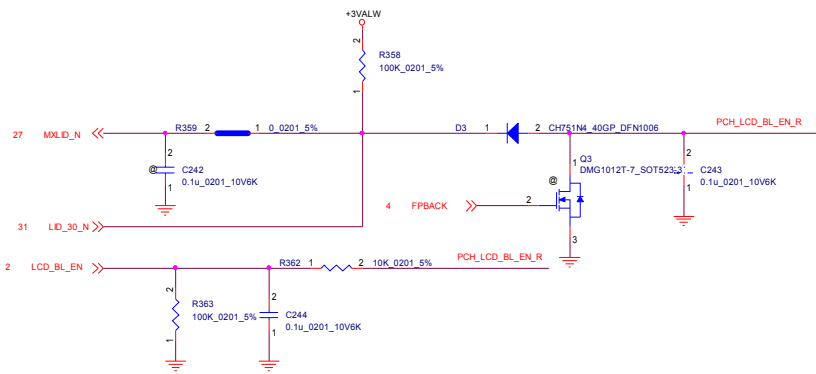
LENOVO.CRDN			
Title			
NGFF SSD			
Size	Document Number	Rev	
C	YOGA930	V1.0	
Date: Wednesday, June 13, 2018			
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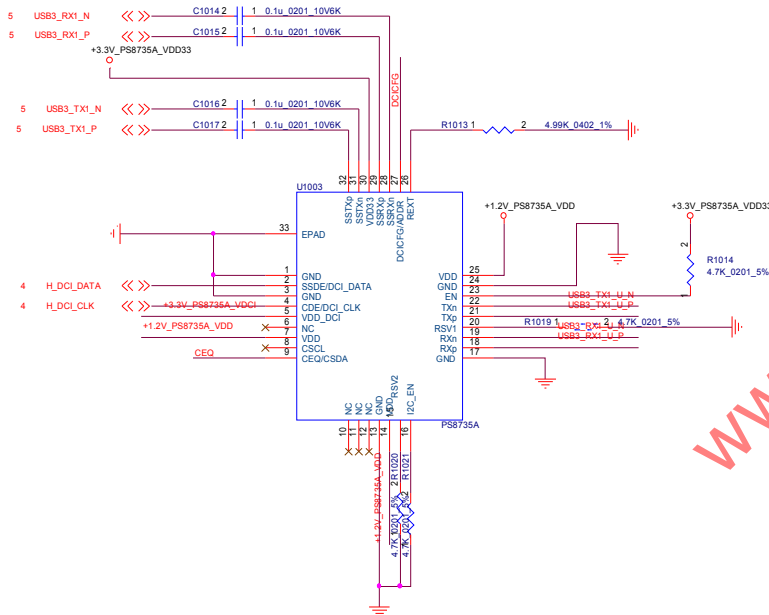
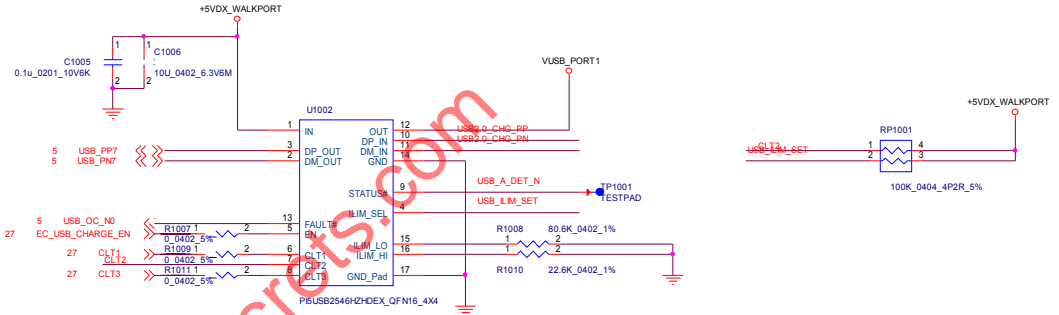
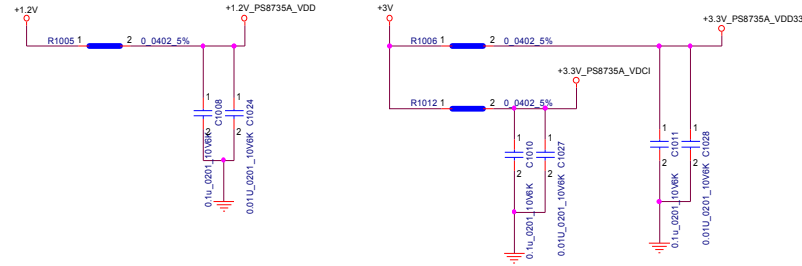
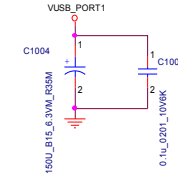
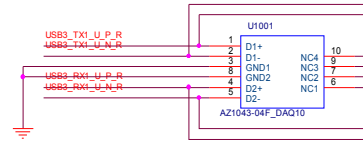
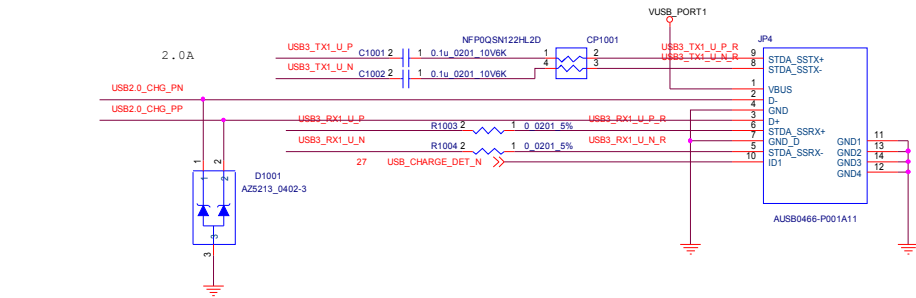
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Title ThermalSensor			
Size C	Document Number YOGA930		Rev V1.0
Date: Wednesday, June 13, 2018 Sheet 22 of 50			
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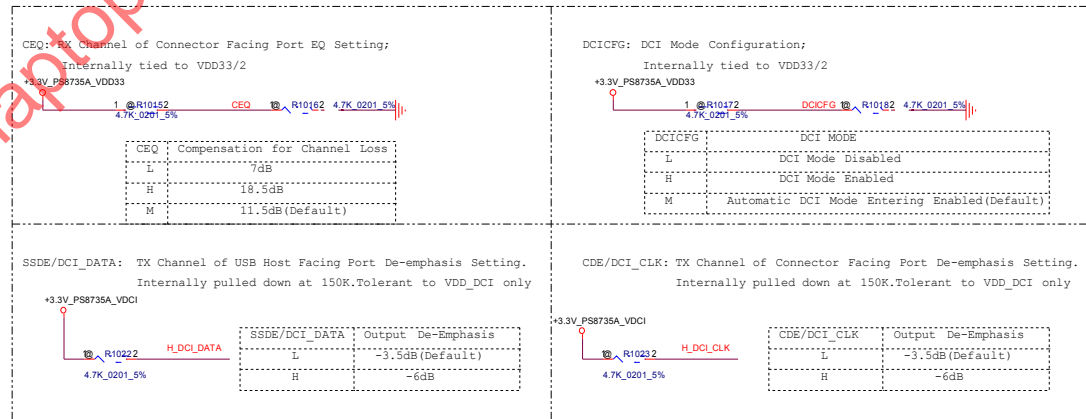
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SENSOR			
Size	Document Number	RevV1.0	
C	YOGA930		
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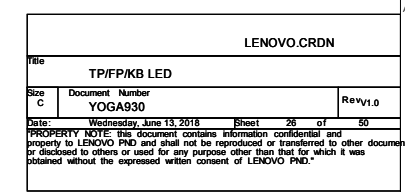
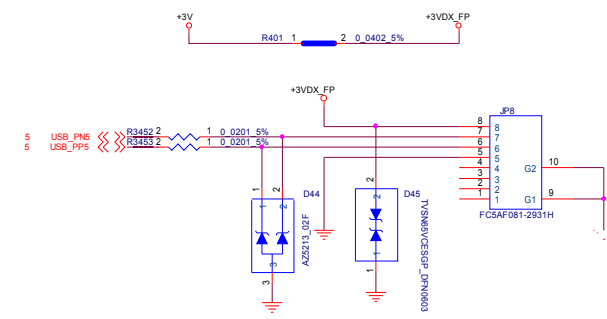
LENOVO.CRDN			
File			
EDP/CAMERA			
Size	Document Number	Rev	
C	YOGA930	V1.0	
Date:	Wednesday, June 13, 2018	Sheet 24 of 50	
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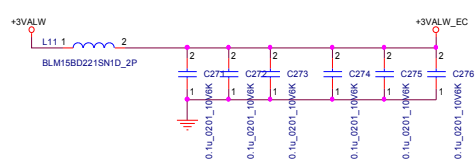


Install ILIM_SEL shunt for ILIM = ILIM_L0 = 0.63A
 Remove ILIM_SEL shunt for ILIM = ILIM_HI = 2.3A
 Support Mouse/Keyboard wake up.
 Support Power Wake
 CLT1 0 -- SDP
 CLT3 1 -- DCF/Auto

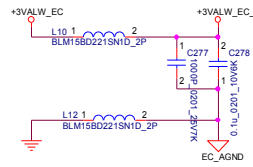


LENOVO.CRDN			
Title			
USB 3.0			
Size	Document Number	Rev	
C	Yoga930	V1.0	
Date	Wednesday, June 13, 2018	Sheet	25 of 50
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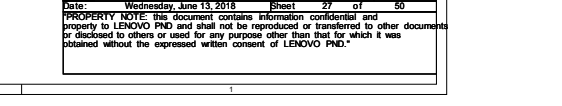
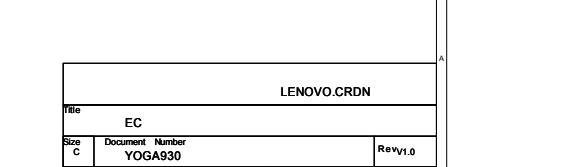
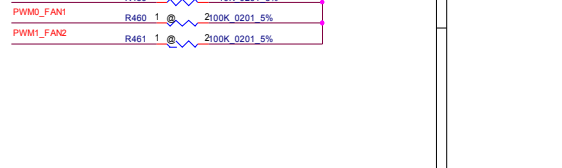
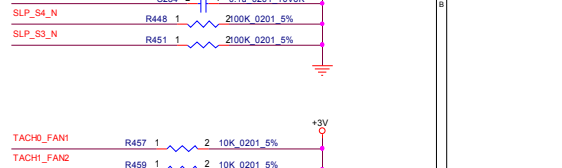
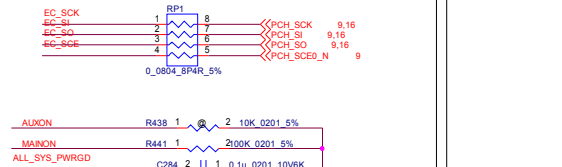
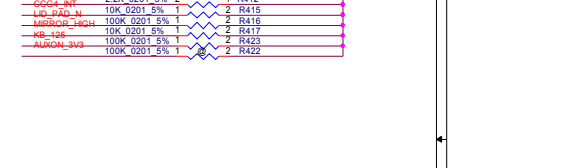
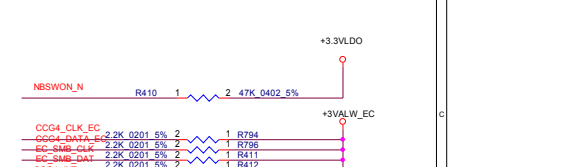
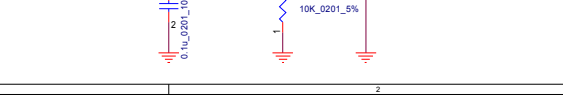
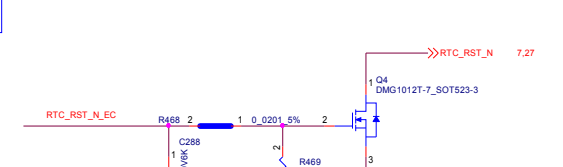
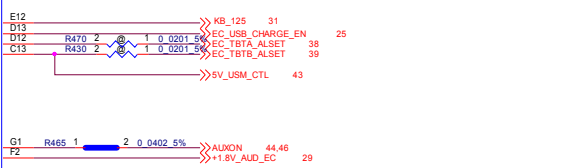
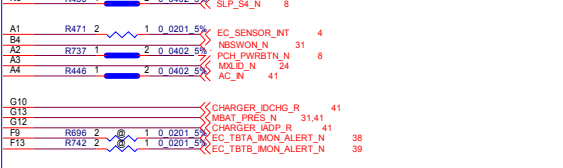
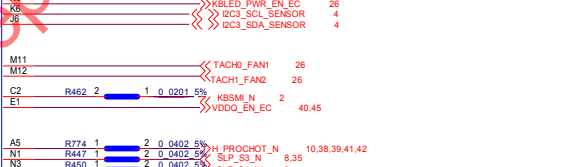
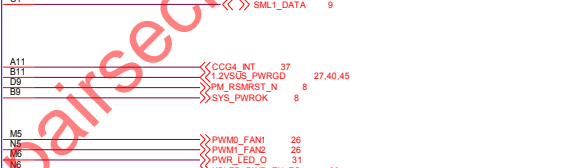
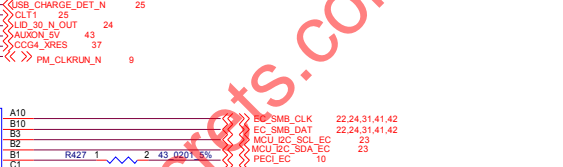
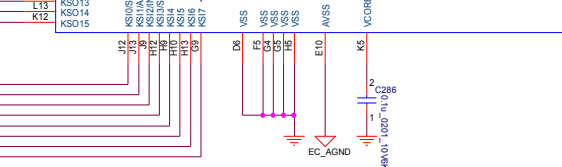
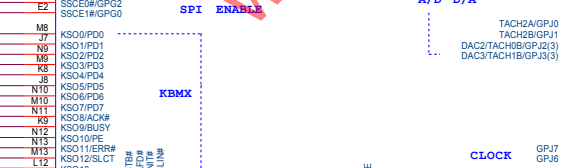
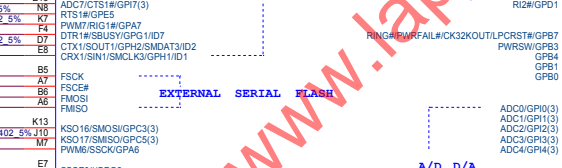
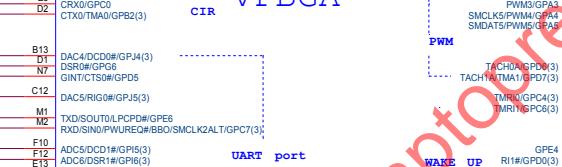
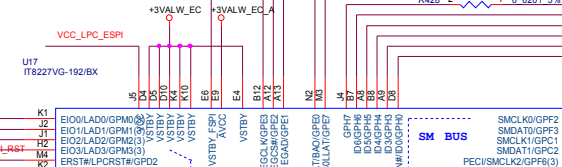
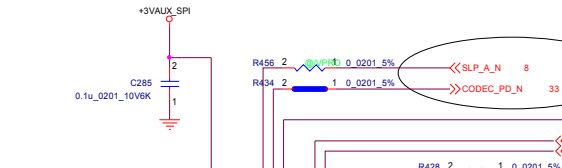
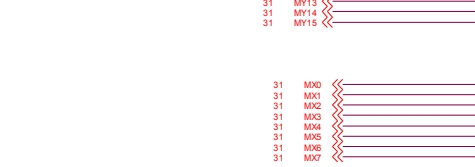
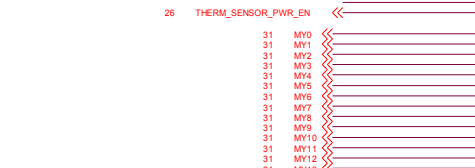
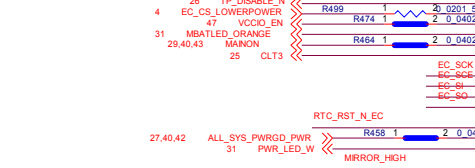
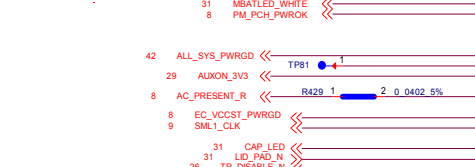
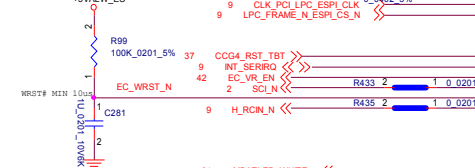
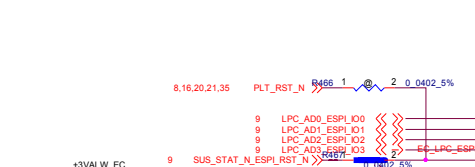
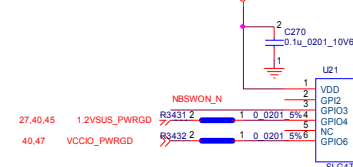
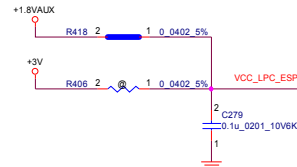




Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.



* Recommended net "+3VAUX" and "RTCVCC" minimum trace width 12mils.



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IT8227 VFBGA

CIR

UART port

EXTERNAL SERIAL FLASH

SPI ENABLE

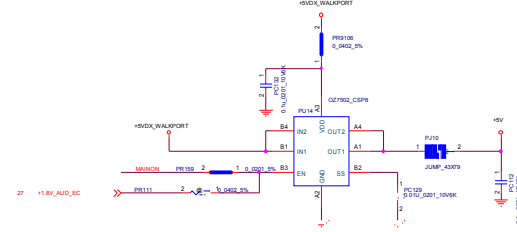
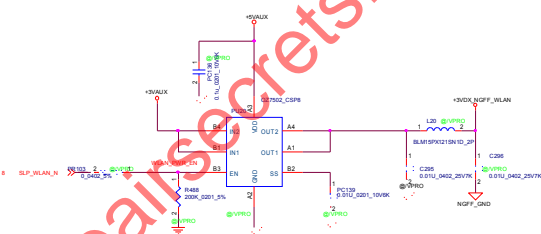
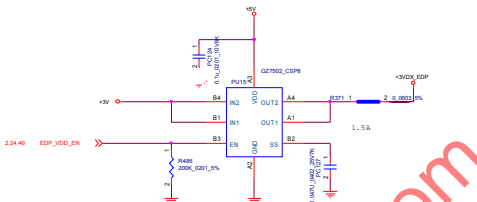
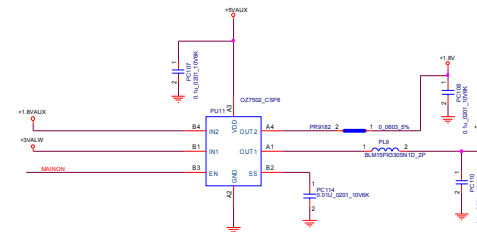
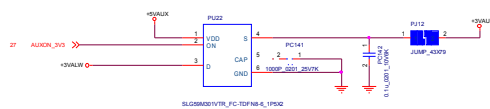
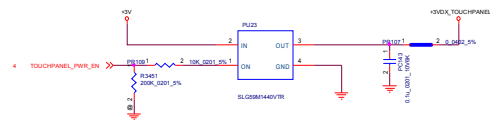
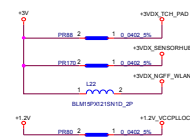
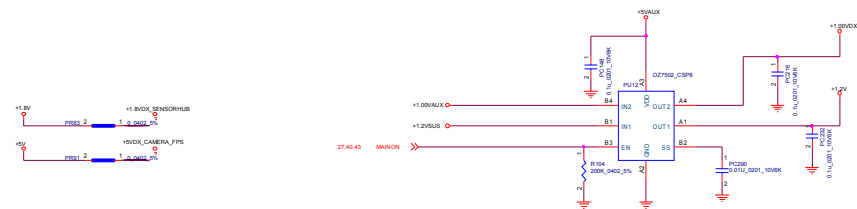
KBMX

CLOCK

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Title			
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C	YOGA930		
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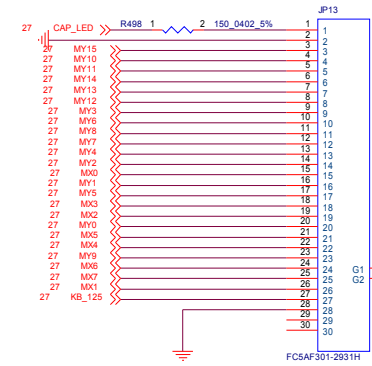
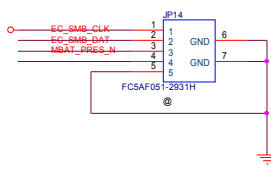
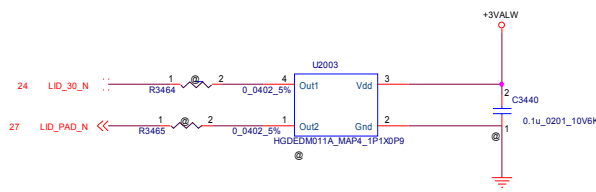
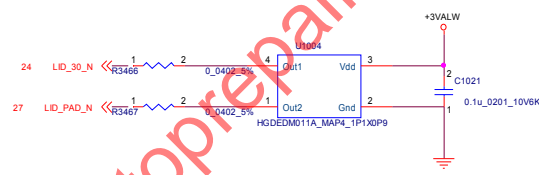
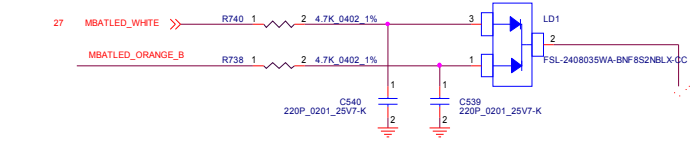
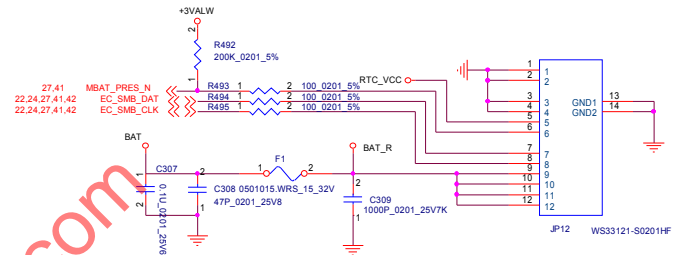
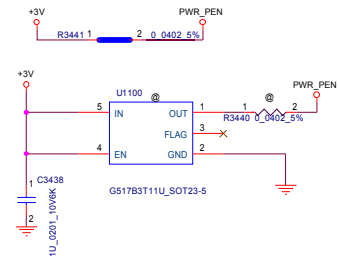
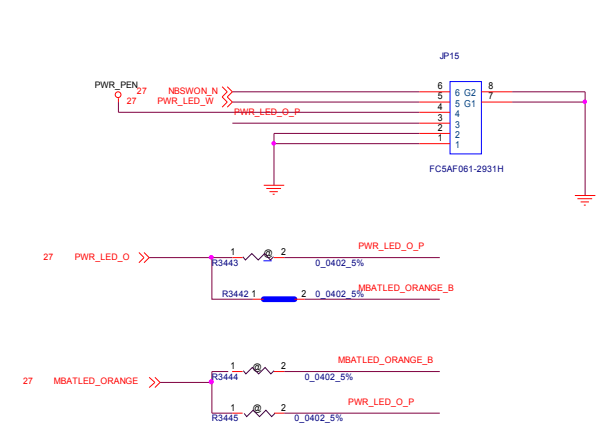


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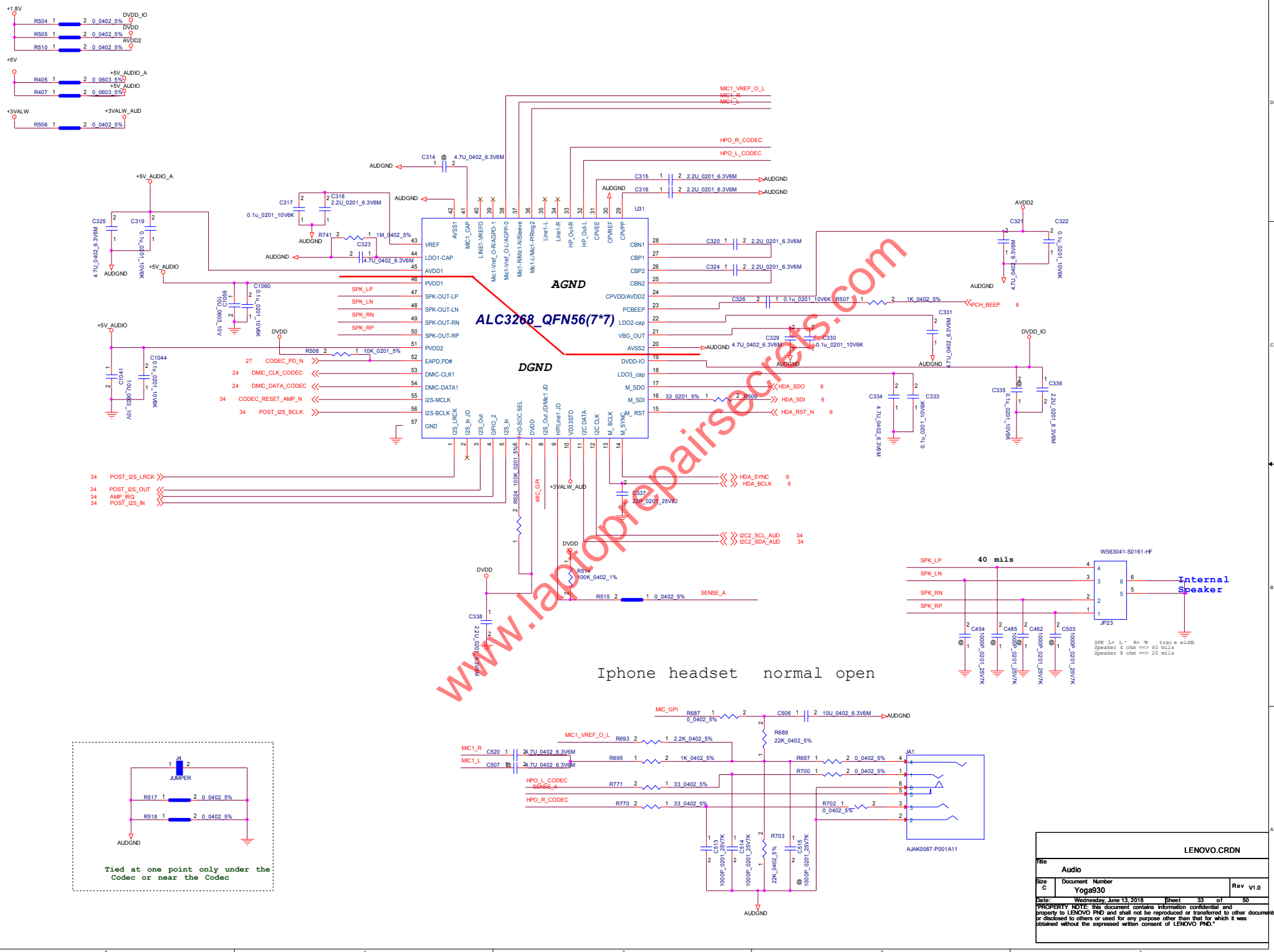
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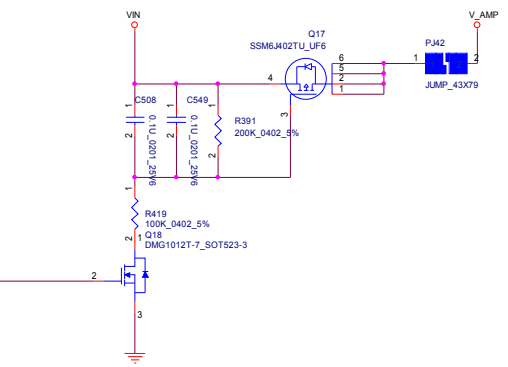
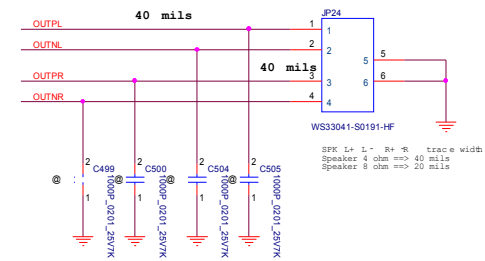
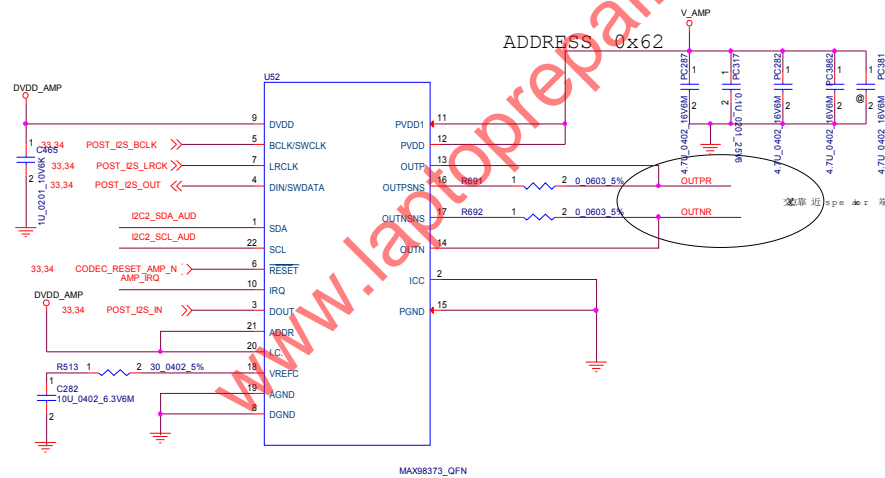


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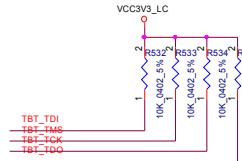
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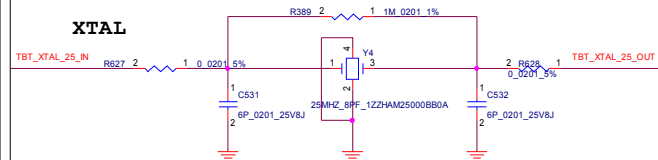
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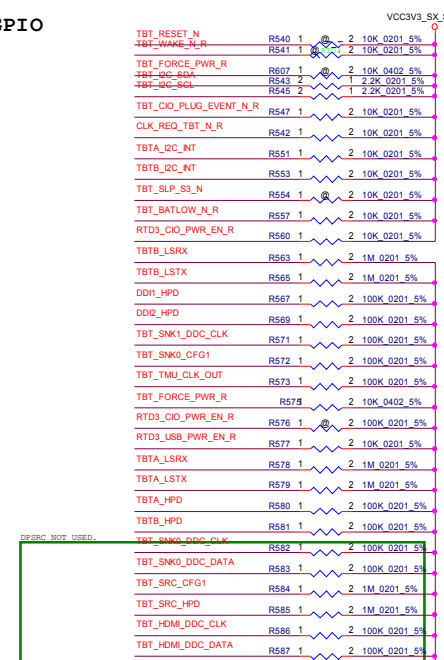
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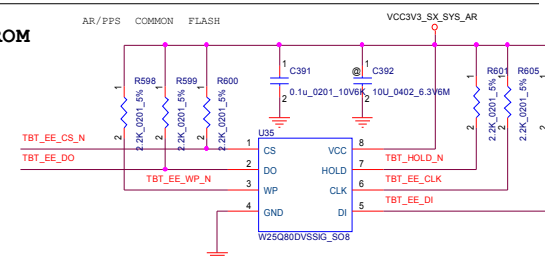
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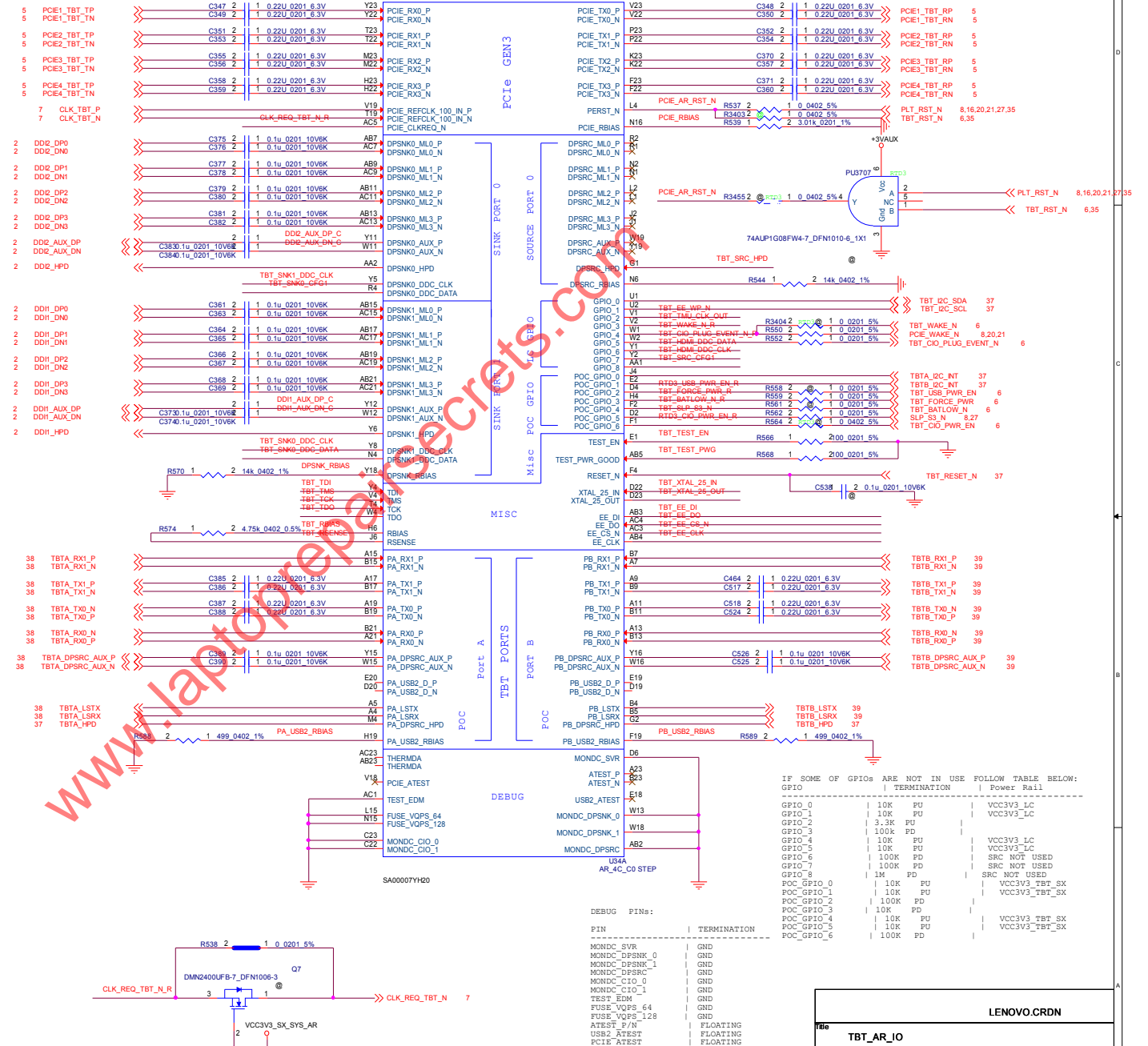
GPIO



ROM



AR-DP TYPE C +USB 3.1 6.0



IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATOR	Power	Resistor
GPIO_0	10K	PU	VCC3V3_LC
GPIO_1	10K	PD	VCC3V3_LC
GPIO_2	3.3K	PU	VCC3V3_LC
GPIO_3	100K	PD	VCC3V3_LC
GPIO_4	10K	PU	VCC3V3_LC
GPIO_5	10K	PD	VCC3V3_LC
GPIO_6	100K	PD	SRC NOT USED
GPIO_7	100K	PD	SRC NOT USED
GPIO_8	10K	PD	SRC NOT USED
POC_GPIO_0	10K	PU	VCC3V3_TBT_SX
POC_GPIO_1	10K	PU	VCC3V3_TBT_SX
POC_GPIO_2	100K	PD	VCC3V3_TBT_SX
POC_GPIO_3	10K	PD	VCC3V3_TBT_SX
POC_GPIO_4	10K	PU	VCC3V3_TBT_SX
POC_GPIO_5	100K	PD	VCC3V3_TBT_SX

DEBUG PINs:

PIN	TERMINATION
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
PCIE_ATEST	FLOATING

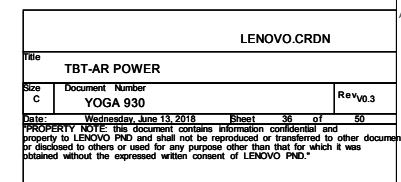
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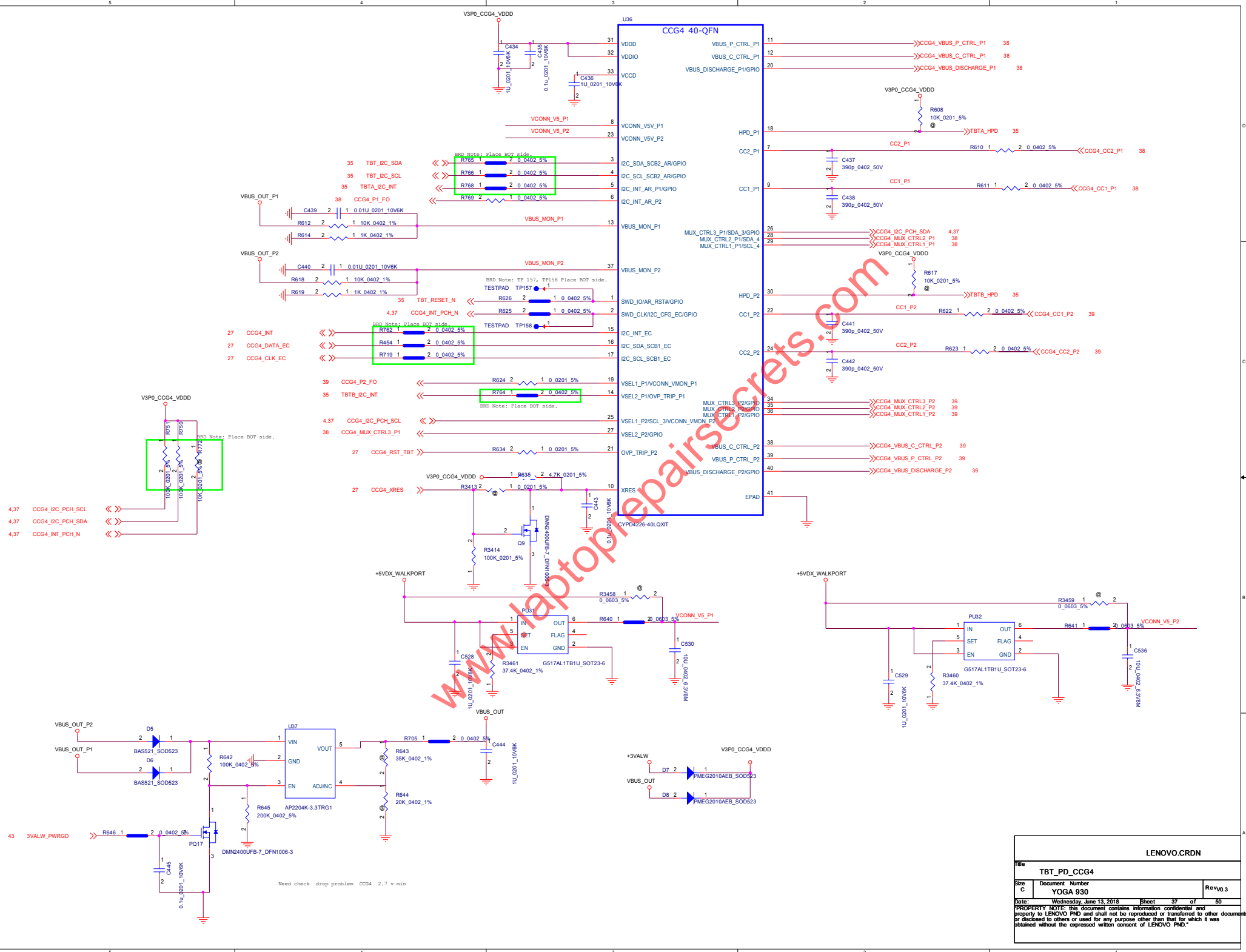
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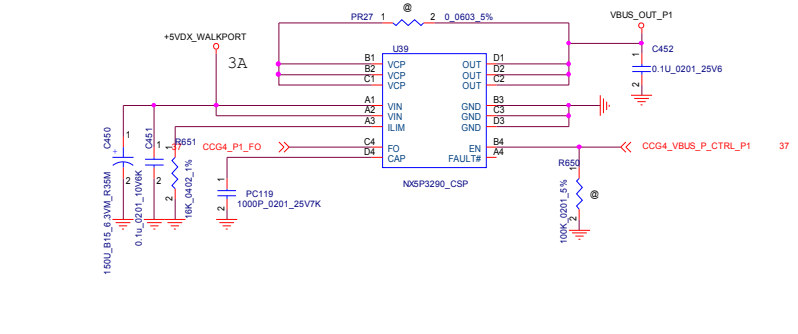
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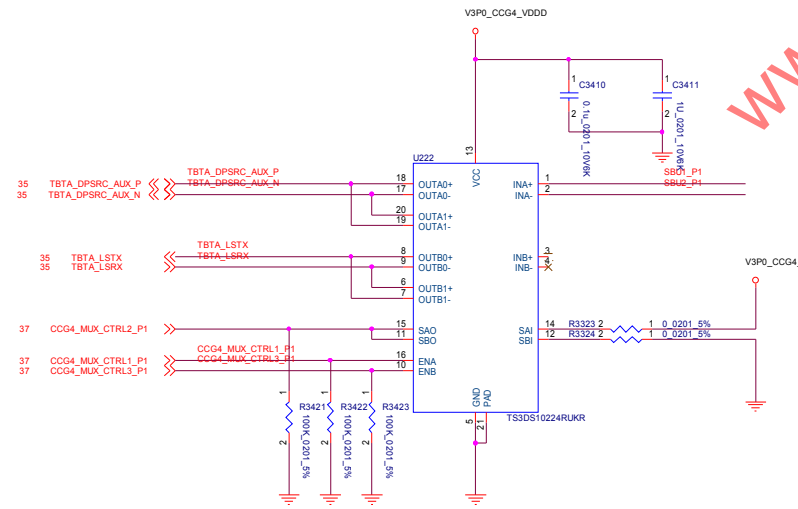
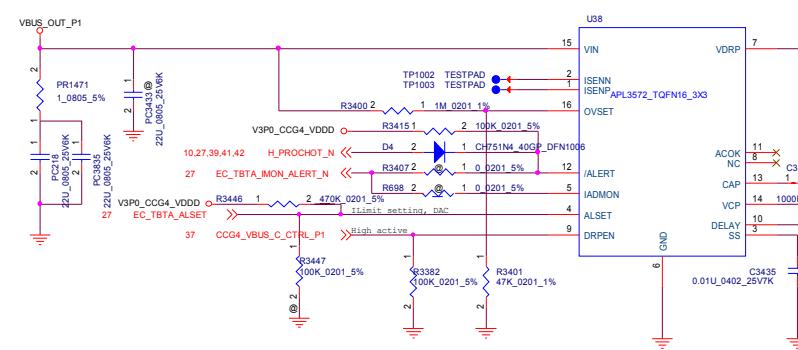
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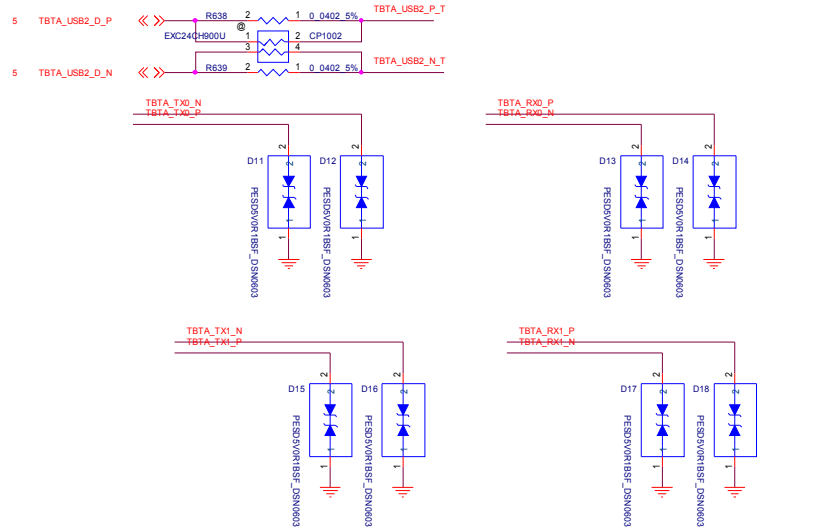
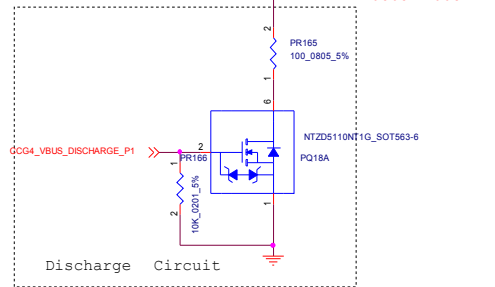
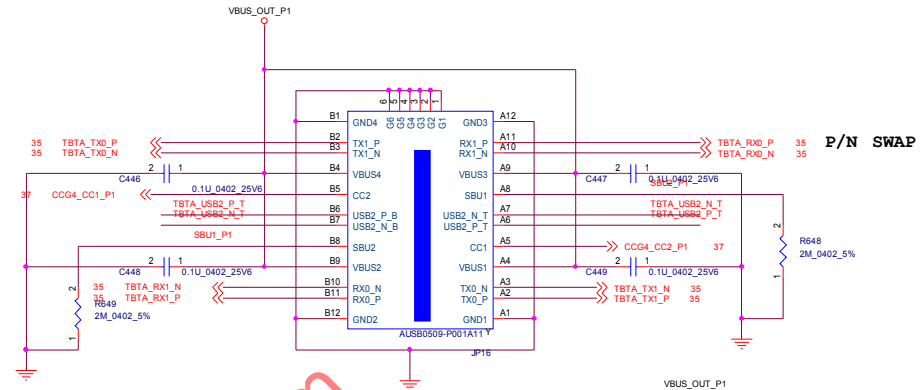




Over Voltage Lock Out Trip Threshold = $1 * (1 + R3400 / R3401)$

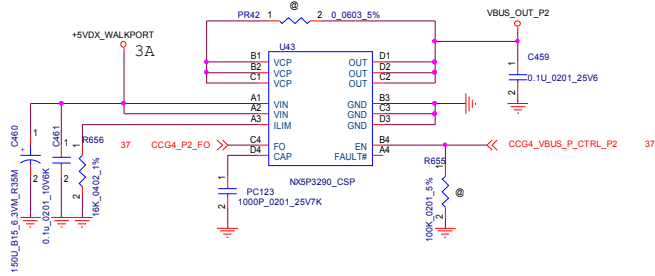


P/N SWAP

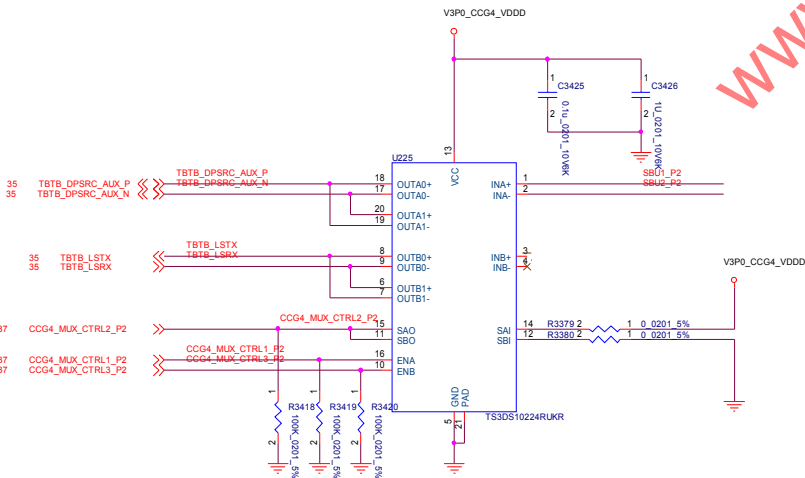
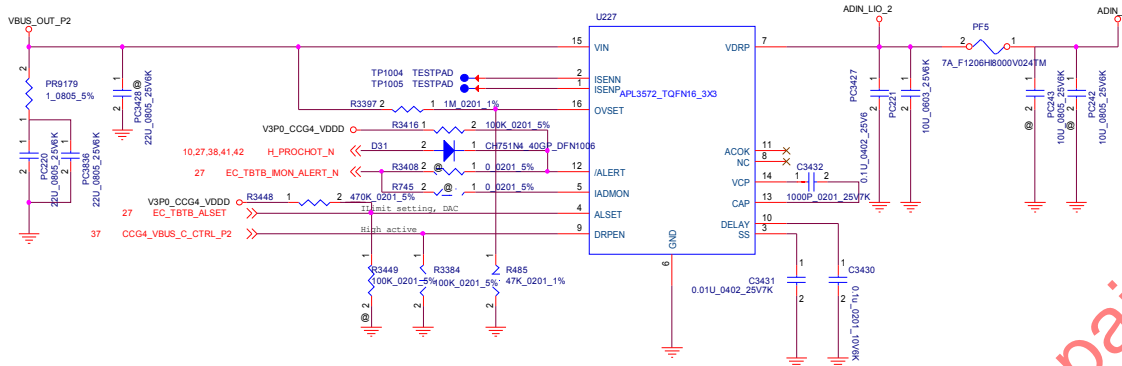


New ESD solution will change

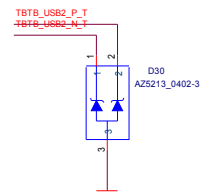
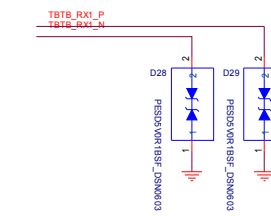
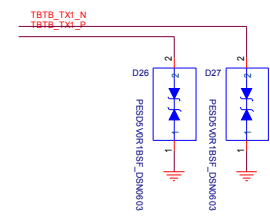
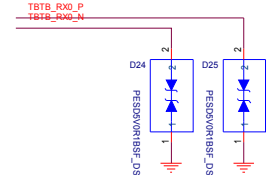
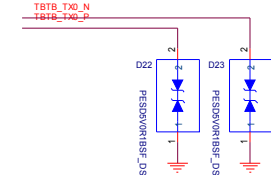
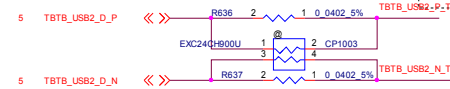
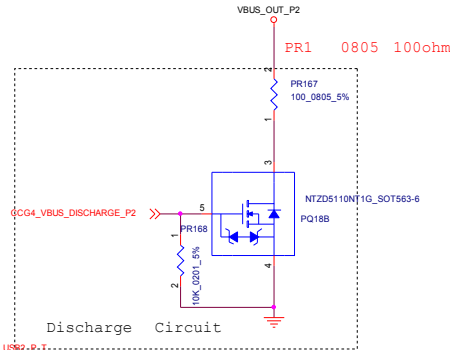
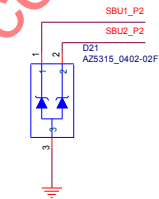
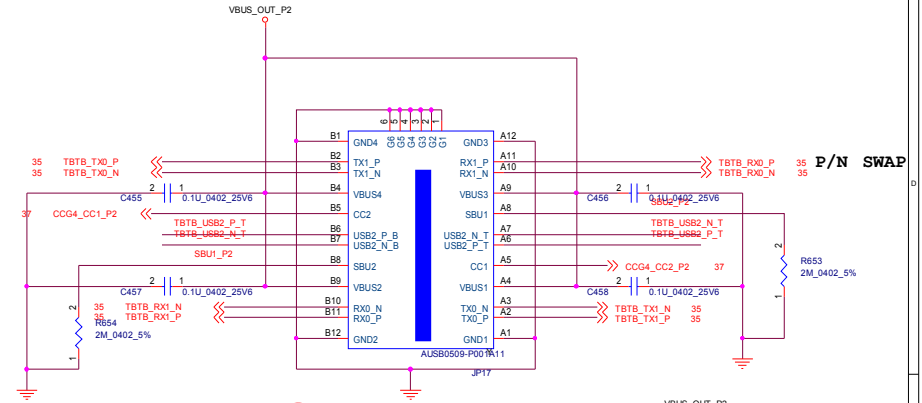
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38 of 50			
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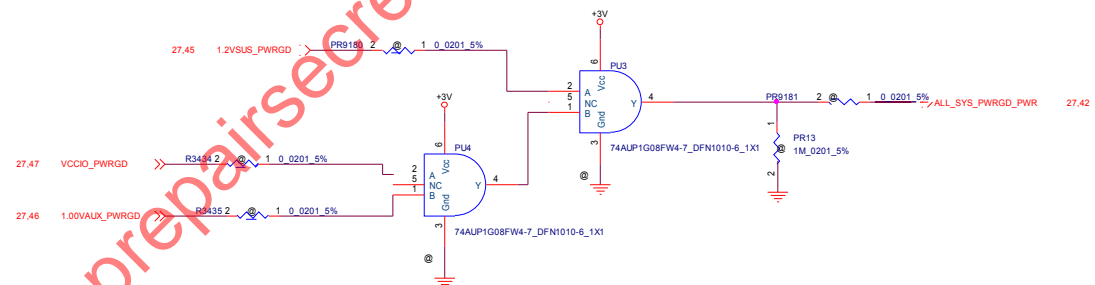
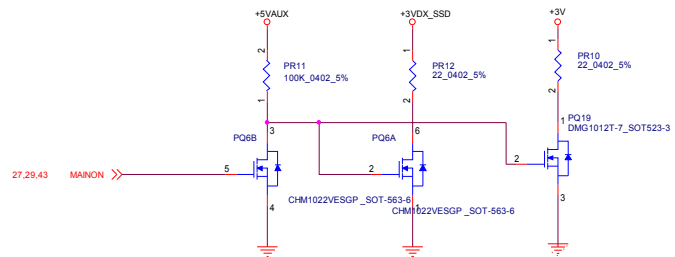
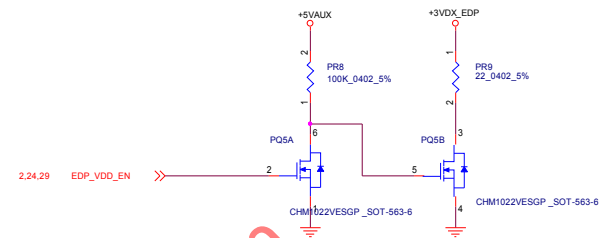
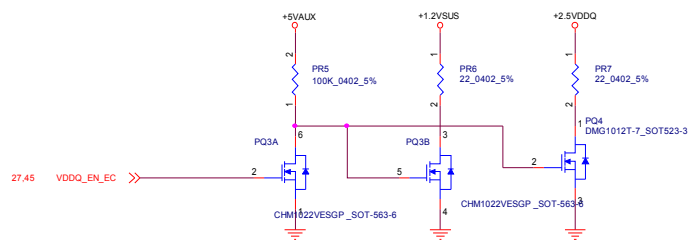
Over Voltage Lock Out Trip Threshold = $1 \cdot (1 + R3397 / R485)$



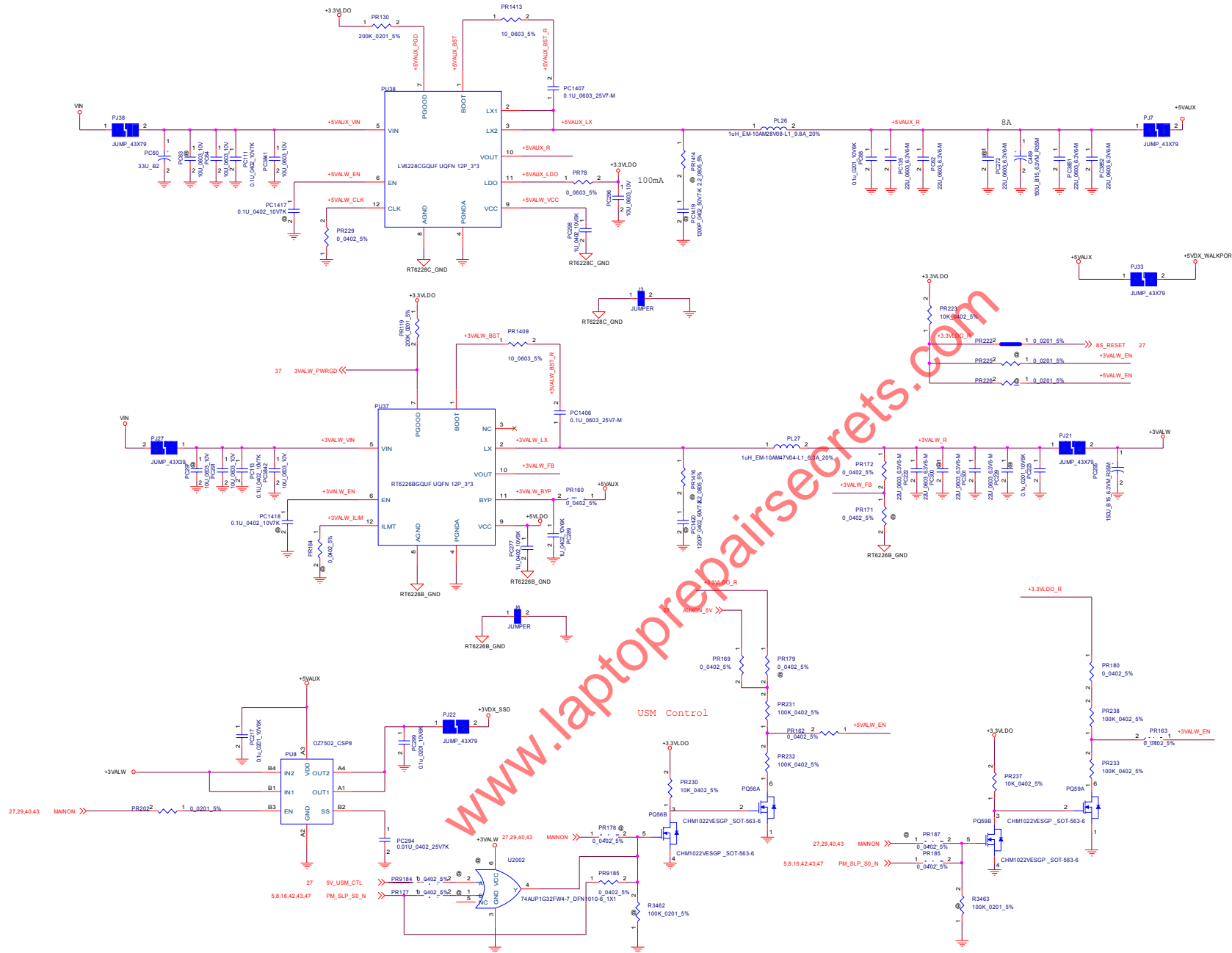
P/N SWAP



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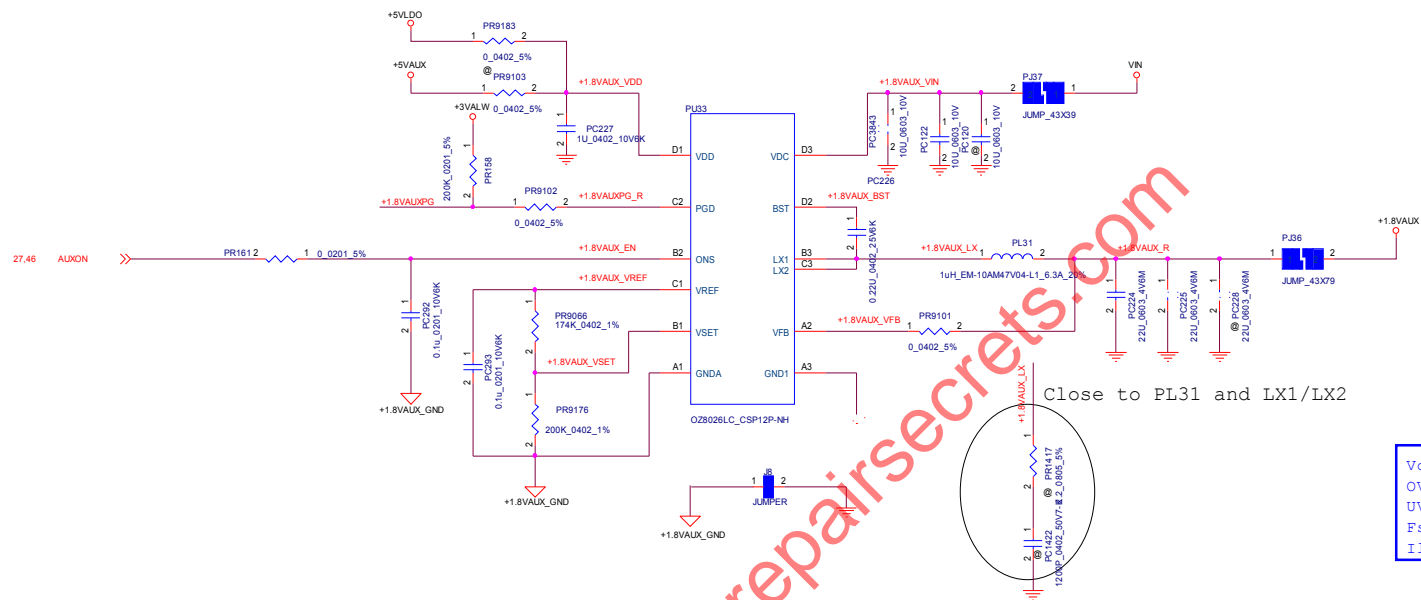
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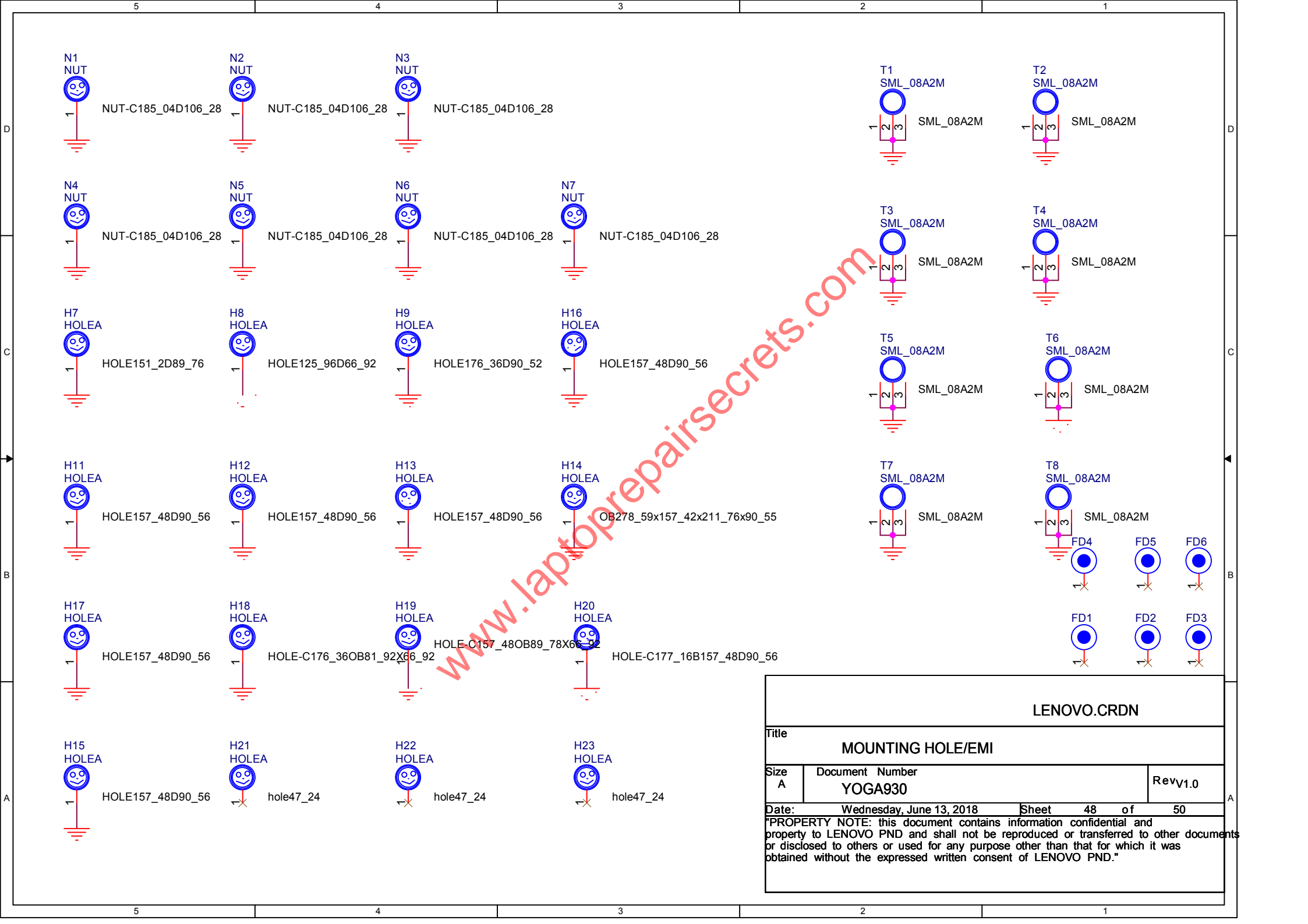
$$\begin{aligned} V_{out} &= 5.1V \\ OVP &= (1.15 - 1.25) * V_{out} \\ UVP &= 0.6 * V_{out} \\ F_{sw} &= 750KHz \\ I_{lim} &= 9A \end{aligned}$$

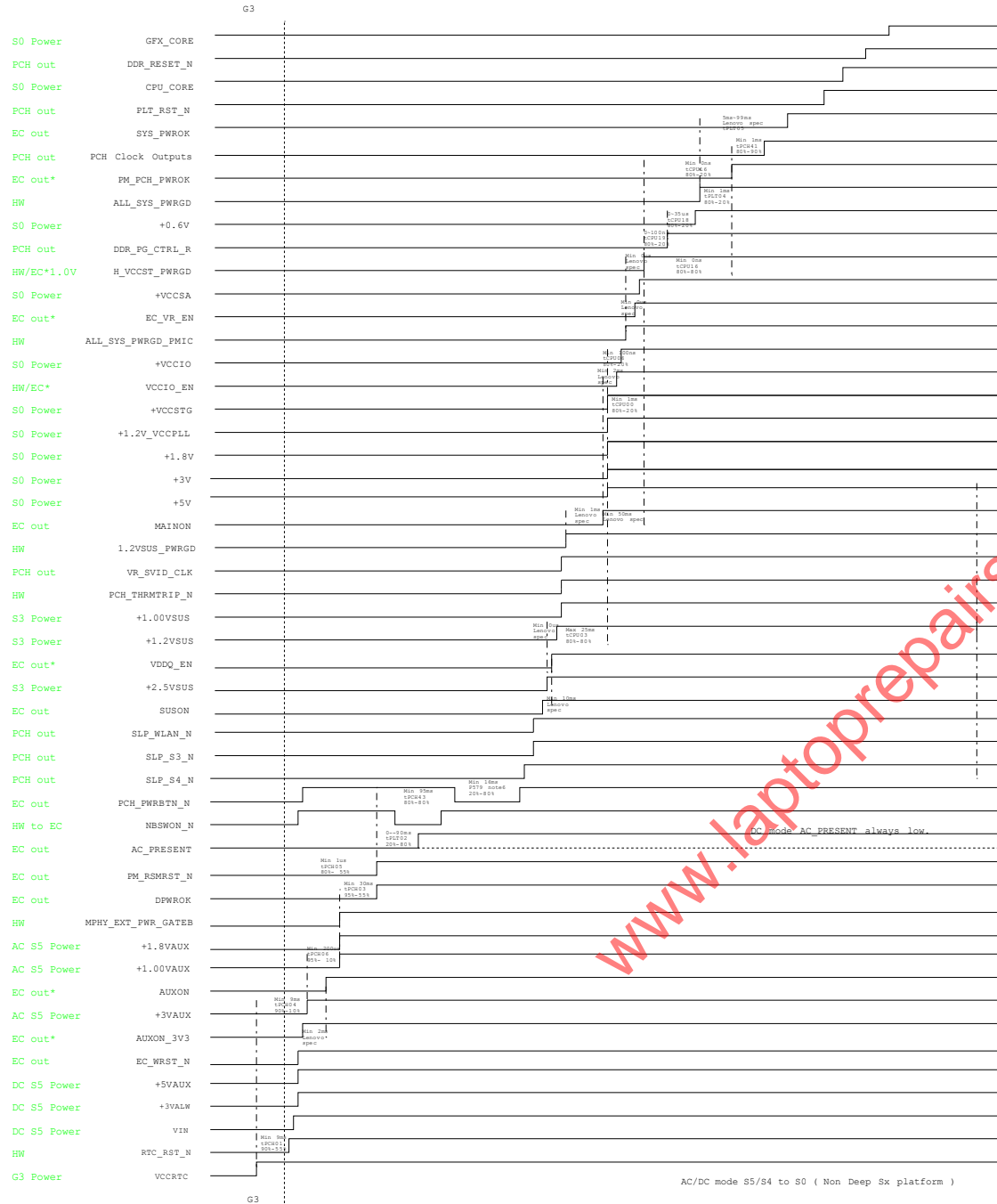
$$\begin{aligned} V_{out} &= 3.3V \\ OVP &= (1.15 - 1.25) * V_{out} \\ UVP &= 0.6 * V_{out} \\ F_{sw} &= 500KHz \\ ILIM &= \text{floating to set current limit } 6A \end{aligned}$$

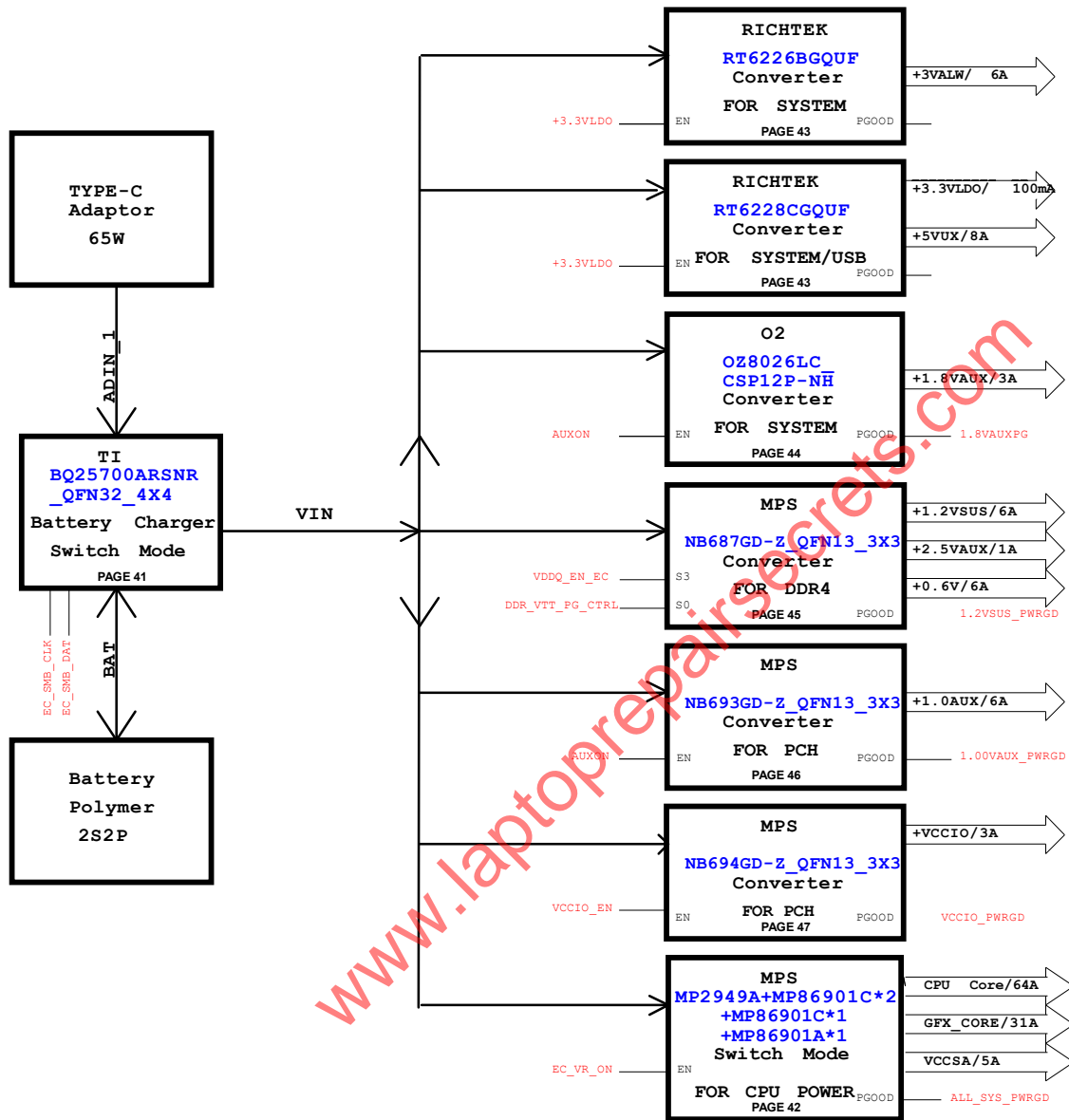
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File	PWR_+3V_LW+5V_AUX			
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$V_{out} = 3.4V \cdot R2 / (R1 + R2) = 1.82V$
 $OVP = V_{out} + 150mV$
 $UVF = V_{out} - 150mV$
 $Fsw = 1000Khz$
 $I_{lim} = 8A$







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